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Atomic layer deposition assisted pattern transfer technology for ultra-thin block copolymer films

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ABSTRACT

As an emerging developing technique for next-generation lithography, directed self-assembly (DSA) of block copolymer (BCP) has attracted numerous attention and has been a potential alternative to supplement the intrinsic limitations of conventional photolithography. In this work, the self-assembling properties of a lamellar diblock copolymer poly(styrene-b-methylmethacrylate) (PS-b-PMMA, 22k-b-22k, L_0 = 25 nm) on Si substrate and an atomic layer deposition (ALD)-assisted pattern transfer technology for the application of DSA beyond 16/14 nm complementary metal oxide semiconductor (CMOS) technology nodes, were investigated. Firstly, two key processing parameters of DSA, i.e. annealing temperatures and durations of BCP films, were optimized to achieve low defect density and high productivity. After phase separation of BCP films, self-assembling patterns of low defect density should be transferred to the substrate. However, due to the nano-scale thickness and the weak resistance of BCP films to dry etching, it is nearly impossible to transfer the BCP patterns directly to the substrate. Therefore, an ALD-based technology was explored in this work, in which deposited Al_2O_3 selectively reacts with PMMA blocks thus hardening the PMMA patterns. After removing PS blocks by plasma etching, hardened PMMA patterns were left and transferred to underneath SiO_2 hard mask layer. Using this patterned hard mask, nanowire array of 25 nm pitch were realized on Si substrate. From this work, a high-throughput DSA baseline flow and related ALD-assisted pattern transfer technique were developed and proved to have good capability with the mainstream CMOS technology.

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1. Introduction

According to the 2013 edition of the international technology road map for semiconductors, directed self-assembly (DSA) of block copolymers (BCPs) has been one of the potential solutions for the next-generation lithographic techniques as well as extreme ultraviolet lithography [1,2], nano-imprint lithography [3,4] and mask-less lithography [5,6]. Being similar with the current mainstream side-wall lithography [7,8], which uses self-aligned side walls as etching masks to create nanofeatures on substrates, DSA uses self-assembling block copolymers as etching masks. Both of them have inherent advantages of low cost and high throughput on fabricating ordered and uniform nanostructures in semiconductor devices [9–11]. For example, fins and gates in FinFET transistors [12,13]. However, as the technology node of semiconductor is being pushed down to 16/14 nm and below [14], side-wall lithography must be combined with double, triple or even quadruple patterning to realize feature patterns of high density, while DSA could satisfy the requirement by its inherent ultra-small periods without additional processes. Pattern transfer is one of the most important processes in DSA technique due to its high relevance with pattern fidelity and defectivity. However, directing pattern transfer from BCP films to substrates was proved to be very challenging for two main reasons. The first one is the low etch resistance of BCP films, whose thickness were usually around several tens of nanometers, which are too thin to withstand effective dry etching in device fabrication. The second one is the poor etch selectivity between two blocks of BCP films. For instance, in the most common used PS-b-PMMA, the etching selectivity between polystyrene (PS) and polymethylmethacrylate (PMMA) under oxygen plasma is approximately 2:1 [15]. Whilst the PMMA is removed, the thickness of remaining PS is pretty thin. Therefore, a method to enhance the resistance of either PS or PMMA in oxygen plasma is needed for the purpose of pattern transfer in device fabrication. In this work, we demonstrate an atomic layer deposition (ALD) assisted pattern transfer technology. In this technology, the PMMA blocks in PS-b-PMMA are selectively hardened which are not easily attacked by oxygen plasma. In combination with a SiO_2 hard mask layer to improve the pattern fidelity and reduce defects as well as control the metal ion contamination, the pattern transfer of hardened PMMA blocks to Si substrate is achieved and Si nanowire array of 25 nm pitch was realized in this work.

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Table 1
Plasma etching parameters.

Process name	Gas chemistries	Gas flow(sccm)	Source Power (W)	Bias (V)	Duration (s)
PS removal	O_2	20	250	−50	60
Break through	$BCl_3/Cl_2/O_2$	10(BCl_3) 5(Cl_2) 5(O2)	250	−50	20
Hard mask etching	$CF_4/CH_2F_2/Ar$	30(CF_4) 10(CH_2F_2) 150(Ar)	250	−140	20
Substrate etching	HBr/O_2	50(HBr) 2(O_2)	250	−50	50

2. Experimental details

2.1. Materials

A random copolymer, poly(styrene-*co*-methylmethacrylate-*co*-hydroxyethyl methacrylate) [denoted as P(S-r-MMA-r-HEMA), M_n = 35 600 kg mol^{-1}, PDI = 1.28, PS mole fraction 57%, HEMA mole fraction = 2%], and a lamellar forming diblock copolymer poly(styrene-*b*-methyl methacrylate) (denoted as PS-b-PMMA, M_n = 22 000-*b*-22 000 kg mol^{-1}, PDI = 1.09), were purchased from Polymer Source Inc. and used without any further purification.

2.2. Preparation of PS-b-PMMA films

Firstly, an 8-nm-thick SiO_2 hard mask was deposited onto the bare silicon wafer by plasma enhanced chemical vapor deposition (PECVD). After that, random copolymer P(S-r-MMA-r-HEMA) solutions of 0.5 wt% in toluene were spin-coated onto the wafer and annealed under vacuum at 240 °C for 5 min to obtain a grafted neutral layer which wets PS and PMMA equally [16]. Ungrafted random copolymers were removed with toluene under ultrasonication for 10 min. Afterward, PS-b-PMMA solutions of 0.7 wt% in toluene were spin-coated onto the neutralized surface, then annealed under vacuum at a temperature above the glass transition temperatures of both PS and PMMA, to induce phase separation of the BCP films. Thicknesses of the BCP films were controlled around 25 nm, which is equal to the natural bulk period (L_0) of the BCP, to avoid the hole-and-island effect in BCP films [17].

2.3. ALD-assisted pattern transfer

The wafers with phase-separated BCP films were put into an ALD chamber and exposed under trimethyl aluminum (TMA) vapor and H_2O vapor at 130 °C for 10 cycles. The exposing times of TMA/purge/H_2O/purge were 30/60/30/60 s respectively. During ALD process, Al_2O_3 molecules were selectively grafted onto the backbones of PMMA chains by reacting with carbonyl groups in PMMA blocks thus hardened them, while no graft occurred in PS blocks due to the lack of chemically active groups e.g. carbonyl groups in PS blocks [18].

A LAM TCP9400 SFM etching tool working at inductive coupling high frequency plasma mode was used for the subsequent dry etching. Firstly, unhardened PS blocks were removed by oxygen plasma etching, followed by a short breaking through step with a BCl_3/Cl_2 gas source. Then, the hardened PMMA patterns were transferred to the underlying SiO_2 hard mask with a $CF_4/CH_2F_2/Ar$ gas source. The residual PMMA blocks were removed by piranha solutions (30% H_2O_2-H_2SO_4 1:5 *v*/*v*) and the left SiO_2 hard mask was used to pattern Si substrate. Finally, Si nanowire arrays of 25 nm pitch were fabricated by plasma etching with a HBr/O_2 gas source. Detailed parameters of the etching processes were shown in Table 1.

3. Result and discussion

3.1. Process optimization of BCP annealing

Phase separation of BCP can be induced through many kinds of methods. Besides the common used thermal annealing and solvent annealing, other methods like laser annealing [19,20] and microwave annealing [21,22] have been developed to meet different specific demands. Generally, thermal annealing is still the most widely used method in semiconductor fabrication due to its good feasibility and compatibility with CMOS flow. Therefore, defectivity and productivity are two very significant considerations for thermal annealing process. We performed some optimization work on our BCP self-assembly process in this part.

Fig. 1 is a schematic diagram of our process flow for self-assembly process of the BCP film on the surface of SiO_2 hard mask. Firstly, a SiO_2 hard mask of 8 nm thickness was deposited onto the bare Si wafer by PECVD. Secondly, the surface of the hard mask was neutralized by grafting P(S-r-MMA-r-HEMA) onto it, so that it can wet both PS and PMMA equally to form perpendicular structures during thermal annealing. Thirdly, the BCP film was spin-coated onto the neutralized surface and thermally annealed to phase separate.

In order to balance the defectivity and the productivity of this flow, a group of experiments with different annealing temperatures and durations were carried out to find an optimal condition. Fig. 2 shows the scanning electron microscopy (SEM) images of PS-b-PMMA films annealed at three different temperatures (180 °C, 210 °C, 240 °C) for six different durations (5 min, 10 min, 15 min, 20 min, 1 h, 3 h). Frames with four different colors (blue, yellow, green, red) were used to mark

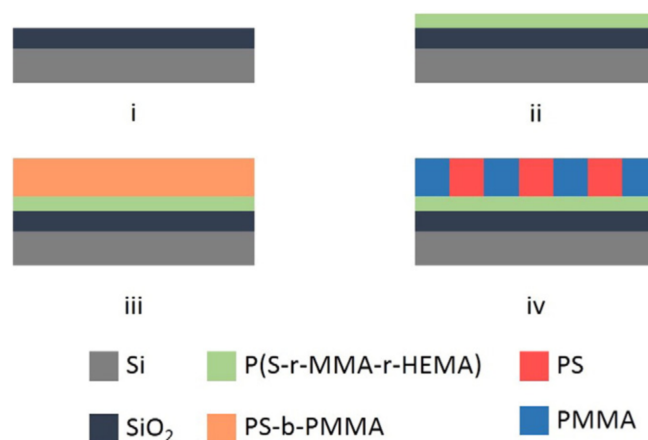

Fig. 1. Schematic representation of the process flow for self-assembly of PS-b-PMMA on the surface of SiO_2 hard mask. (i) SiO_2 hard mask deposition on Si substrate by PECVD; (ii) neutral layer grafting on the surface of SiO_2 hard mask; (iii) spin-coating the PS-b-PMMA film onto the neutralized surface; (iv) phase separation of the BCP film by thermal annealing.

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