Thin Solid Films 613 (2016) 48–54

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Silicon nanowire hot carrier electroluminescence

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ARTICLE INFO

Article history:
Received 13 July 2015
Received in revised form 17 November 2015
Accepted 17 November 2015
Available online 28 November 2015

Keywords:
Silicon-on-insulator
Silicon
Electroluminescence
Nanowire
Hot carriers

ABSTRACT

Avalanche electroluminescence from silicon pn junctions has been known for many years. However, the internal quantum efficiencies of these devices are quite low due to the indirect band gap nature of the semiconductor material. In this study we have used reach-through biasing and SOI (silicon-on-insulator) thin film structures to improve the internal power efficiency and the external light extraction efficiency. Both continuous silicon thin film pn junctions and parallel nanowire pn junctions were manufactured using a custom SOI technology. The pn junctions are operated in the reach-through mode of operation, thus increasing the average electric field within the fully depleted region. Experimental results of the emission spectrum indicate that the most dominant photon generating mechanism is due to intraband hot carrier relaxation processes. It was found that the SOI nanowire light source external power efficiency is at least an order of magnitude better than the comparable bulk CMOS (Complementary Metal Oxide Semiconductor) light source.

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1. Introduction

Avalanche electroluminescence from silicon pn junctions was first reported 60 years ago [1]. However, since silicon is an indirect band gap semiconductor material, the internal quantum efficiency of photon generation is quite low [2]. Over the last two decades silicon light source efficiencies have been improved significantly to the point where some novel applications are seriously being considered [3]. These applications include optical data communication [4,5], near to eye micro-displays [6,7] and optical biosensors [8,9].

The search for efficient light sources in silicon has been described as looking for the Holy Grail of the silicon integrated circuit technology [10]. This search is still on-going and different approaches are followed to realise photon generation in the indirect band gap material. These approaches include [11] silicon nanocrystals embedded in oxide, Er doping of silicon, Si/Ge quantum dots and ion implanted Si in SiO_2. Significant progress has been made towards the realisation of lasers in silicon using a variety of methods [12]. A very interesting approach was to combine silicon nanocrystals incorporated in a silica matrix with Er doping to generate light emission around 1500 nm in silicon, since Er-doped silicon nanocrystals behave as electron–hole pair traps [13].

However, the key to successful commercialisation of any silicon-based light source technology will be to develop a high-volume manufacturing process where light sources can be processed in a CMOS (Complementary Metal-Oxide Semiconductor) fabrication facility alongside existing CMOS wafers in order to amortise their costs [14]. CMOS compatibility is of the utmost performance in order to take advantage of the vast investment in current silicon integrated circuit fabrication facilities.

Several photon generating mechanisms have been proposed for the avalanche electroluminescence light emission form silicon. The main contenders are direct and indirect intraband transitions of hot carriers, as well as the indirect interband recombination of carriers. The intraband transitions can be direct or indirect, with the indirect transitions either phonon assisted (PA) or ionised impurity assisted (IA). The IA transitions are also referred to as Bremsstrahlung. The Bremsstrahlung origin of the hot-carrier-induced light emission was critically reviewed [15] with the eventual conclusion that Bremsstrahlung cannot be considered as a major contributor to photon generation. It was concluded that electron energy relaxations between states of the conduction bands (c–c) are the most likely processes responsible for the hot-carrier-induced luminescence in silicon. Using an innovative double gate MOS transistor structure [16], it was also concluded that direct and indirect phonon assisted (PA) intraband transitions appear to be the dominant emission mechanisms in silicon.

In this study we aim to improve the external quantum and power efficiencies of a silicon avalanche electroluminescent pn junction light source. This can be achieved by i) lowering the operating voltage, and ii) increasing the light extraction efficiency. The structures under investigation were light emitting pn junctions manufactured within an active silicon thin film layer on top of a silicon dioxide (buried oxide or BOX) layer. A custom SOI (silicon-on-insulator) processing sequence was designed to realise the nanowire structures. The reverse bias technique of reach-through was also used to modify the electric field distribution in the junction depletion region and lower the operating voltage. Thin silicon films with an active layer thickness of less than 50 nm were realised and nanowires with diameters of less than 50 nm and lengths

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http://dx.doi.org/10.1016/j.tsf.2015.11.045
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varying from 150 nm to 600 nm were manufactured within the thin silicon film. Of special interest when characterising the devices were the spectral emission properties, the operating voltages and the device efficiencies.

2. Device structures and biasing

The device structures under investigation were i) pn junctions formed in a continuous thin film silicon layer, and ii) pn junctions formed in a large number of parallel nanowires within the thin silicon layer. These pn junctions were biased in the reach-through region of operation.

2.1. Reach-through devices

Reach-through devices have a single pn junction structure, schematically shown as an n^+pp^+ diode in Fig. 1. The electric field distribution E(x) is shown along the length of the device. The maximum electric field E_C at the n^+p metallurgical junction constitutes the critical electric field needed to initiate avalanche carrier multiplication. The reach-through separation dimension d_{RT} between the two highly doped regions is also shown. For large d_{RT} values the classic triangular electric field distribution is shown in Fig. 1(a). At smaller d_{RT} dimensions the electric field is truncated at the value E_R at the pp^+ interface because the lightly doped p region between the two highly doped regions is fully depleted.

According to Poisson's law, the reverse bias junction potential will scale directly with the integral of the electric field distribution E(x) over distance, and from Fig. 1(b) it can be observed that smaller separation d_{RT} distances will result in lower operating voltages, thus improving the power efficiency of the device. Another important result is that the average electric field in the depletion region will increase with smaller d_{RT} distances, since the critical electric field E_C to initiate avalanche carrier multiplication will remain almost constant with varying distances d_{RT}. It is important to note that in the reach-through case a large density of carriers will only be achieved under high electric field avalanching conditions.

The voltage drop across the lightly doped p-type depletion region can be calculated as the area under the electric field distribution shown in Fig. 1. In the case of no reach-through in Fig. 1(a) the voltage across the device is given by

$$V(d_C) = V_{p^+n^+} + \frac{1}{2}E_C d_C \quad d_{RT} \geq d_C \tag{1}$$

where

$V_{p^+n^+}$ = voltage drop across the n^+ and p^+ depletion regions,
E_C = critical electric field to cause carrier multiplication and avalanche breakdown,
d_C = depletion region width into p-type region at avalanche with no reach-through, and.
d_{RT} = reach-through separation distance.

Similarly, the area under the electric field in the reach-through condition in Fig. 1(b) gives the voltage across the device as

$$V(d_{RT}) = V(d_C) - \frac{1}{2}E_R(d_C - d_{RT}) \quad d_{RT} < d_C \tag{2}$$

where E_R = The electric field at the reach-through point $x = d_{RT}$.

The linear distribution of the electric field in Fig. 1(a) can be expressed as

$$E(x) = E_C\left(1 - \frac{x}{d_C}\right) \tag{3}$$

and thus

$$E_R = E(d_{RT}) = E_C\left(1 - \frac{d_{RT}}{d_C}\right). \tag{4}$$

By substituting Eqs. (1), (3) and (4) into Eq. (2), the breakdown voltage in reach-through can be approximated by

$$V(d_{RT}) = V_{p^+n^+} + E_C\left(d_{RT} - \frac{d_{RT}^2}{2d_C}\right) \quad d_{RT} < d_C. \tag{5}$$

It should also be noted that Eq. (5) is only valid for separation distance $d_{RT} \leq d_C$. For the no reach-through condition where $d_{RT} > d_C$, Eq. (1) should be used for the breakdown voltage. In Eq. (5), when $d_{RT} = d_C$, the breakdown voltage reduces to Eq. (1).

The above Eq. (5) shows that the operating voltage $V(d_{RT})$ will decrease as the reach-through separation distance d_{RT} is decreased. If the reach-through distance d_{RT} is made longer than d_C, the maximum avalanche operating voltage given in Eq. (1) will be reached, determined mainly by the acceptor doping in the central p-type region.

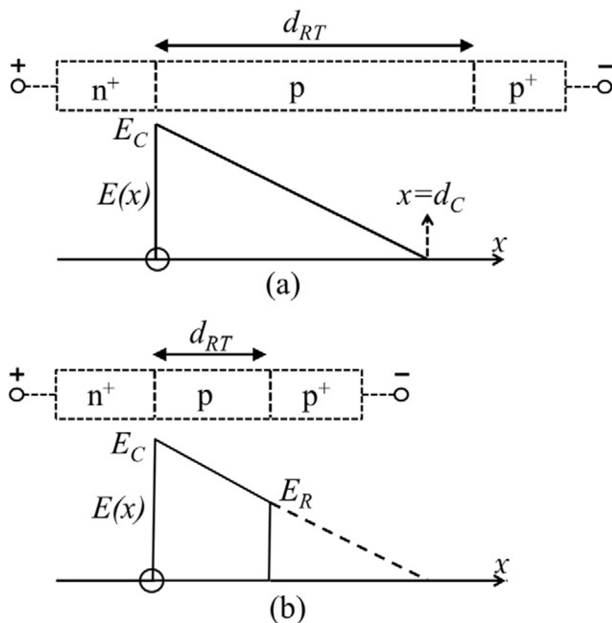

Fig. 1. Electric field distribution in the single junction n^+pp^+ device. (a) Classic junction case, and (b) reach-through condition.

2.2. SOI thin film structure

The SOI starting material was a silicon substrate with a 3 μm thick buried silicon dioxide layer, and a lightly doped p-type single crystal silicon layer (the active layer) with thickness 80 nm on top of the buried oxide (BOX). The device structure of the thin film device is shown in Fig. 2. The first process step was to increase the p-type doping of the active layer by performing a blanket low energy boron implant of dose 1.2×10^{14} ions/cm^2 at an energy of 10 keV. After annealing of the implant, the silicon islands were etched using reactive ion etching (RIE) with plasma enhanced chemical vapour deposition (PECVD) oxide as mask. A PECVD oxide was again used as mask to define the n^+ regions. Arsenic implantation at an energy of 50 keV and dose of 1×10^{15} ions/cm^2 was performed to form the n^+ islands. Silicon nitride was used as local oxidation mask to selectively protect the 80 nm thick n^+ and p^+ islands when a dry thermal oxidation technique was used to thin the material between the islands to a nominal thin film thickness t of approximately 40 nm. In order to have a silicon dioxide layer of

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