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Thermally-induced failures of copper through-silicon via structures evaluated by the strain energy density model

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ABSTRACT

Based on the current density (CD) experimental results reported in a literature for the copper through-silicon vias (TSVs) arising in the Cu/Ti/SiO_2/Si wafer structure, the CD solutions were obtained through simulations in the ANSYS/LS-DYNA software linked with the "Johnson-Cook (J-C) Constitutive Model" module in this study. The numerical schemes are developed to obtain the following contents: (1) the determinations of the unknown coefficients in the J-C model by conducting the microtensile tests for per each component of the TSV structure; (2) the earliest element failure caused by the thermal strain/stress; (3) the critical stress and time at potential failure location modeled by the J-C model; and (4) the evaluations of strain energy density ($W_{failure}$) required for element failures in the components and the effect of heat generation rate in per unit volume of Cu film on element failure. The numerical solutions predicted by the present models are confirmed to be very close to the reported experimental results, and thus validate the present predictions for temperature and time and the sequence of elements with the earliest failure in their component. The strain energy density ($W_{failure}$) required to start the failure of an element is found to be dependent upon the TSV component material only, and is independent of the element's location in the same component. The heat generation in the Cu film is of importance to the order of the TSV components reaching its $W_{failure}$, the time to have $W_{failure}$ increases along with the distance of the TSV component from the lateral surface of the Cu film. The smaller the distance is, the earlier the time that the $W_{failure}$ of an element is reached. An appropriate combination of a Ti film with a large thickness and SiO_2 film with a small thickness can reduce the maximum effective stress (σ_{max}) and provide an efficient barrier for copper diffusion into the Si wafer substrate. This study can provide an efficient method for the design and failure protection of TSV structures.

1. Introduction

Three-dimensional (3-D) interconnects using the through-silicon via (TSV) technology have attracted much attention in the microelectronics industry due to their potential for great improvements in the performance of micro-electric devices, as well as their promise as a joining method for 3-D integrated circuit devices. They also enable advanced multi-level chips integrating complementary metal-oxide semiconductor technologies for use in emerging technologies, such as microelectromechanical systems and bio-chips [1]. One of the key issues in the implementations of 3-D interconnects using TSV is the control of mechanical stresses in the Cu film of the TSV structure and in the surrounding silicon substrate [2,3]. Effective stresses induced by thermal treatment in the TSV interconnect schemes, and stresses induced due to silicon wafer thinning or chip-package interactions, introduce reliability challenges for TSV technology, and the stresses in the Si substrate surrounding the copper-filled TSV can affect electron mobility in the transistors [4].

Efforts to measure stresses in the 3-D TSV structures involve the micro-Raman technique [5,6] and synchrotron x-ray micro-diffraction (XRM) [6,7]. The stresses in the silicon substrate surrounding the Cu TSV and in the Cu TSV can be measured simultaneously. The results suggest that Cu stress may lead to reliability as well as integration issues, while Si stress may lead to device performance concerns. Using XRM, the impacts of such findings on reliability and robust integration of the devices have also been reported [8,9]. The failure of Cu TSV under biased thermal stress was reported in Seo et al. [10]. The time-dependent dielectric breakdown (TDDB) of the oxide liner in the TSV was measured to detect the migration of copper from TSV to silicon. Thermal cracking was caused by the expansion of copper TSV under test conditions. Calibrated micro-Raman spectroscopy and finite element analysis (FEA) are non-destructive methods that can be used to

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determine local silicon stress [11]. The effect of TSV density on local stress concentration had been evaluated, and the design rules for optimal mechanical flexibility in a system were then defined based on these.

Thermo-mechanical reliability is of importance to the development and deployment of TSV technology in 3-D microelectronic packaging. The mismatch in the coefficient of thermal expansion (CTE) between the Cu line and the surrounding TSV components, including the Si wafer, upon temperature variation can affect the overall thermal expansion behavior of the whole TSV structure, and generate an internal stress state. In the study of Cheng and Shen [12], FEA was used to study the effects of in-plane CTE of the Si/Cu composite structure. They also examined the evolution of stress and deformation fields, and identified potential reliability concerns associated with thermal loading. Simulations were applied on the basis of three different TSV models in Tan et al. [13] using FEA modeling. It was found that thermo-mechanical stress is the dominant contributory factor to the electromigration performance in TSV, instead of the current density. The reliability of TSV interconnects and interlayer bonding between the silicon layers are issues that become more complicated in 3-D ICs. Ladani [14] addressed the impact of size design parameters and properties on the thermo-mechanical durability of direct chip attach solder joints and TSV interconnects in a 3-D IC package. The most influential factor on TSV durability was found to be TSV diameter. The location of failures was also found to be a function of effective CTE and the size parameters.

In Liu et al. [15] TSV samples were fabricated and evaluated under thermal-shock testing from −55 °C to 125 °C. The results from the fracture analysis matched the experimental observations, and also provided insights on the reasons behind different failure mechanisms. Udupa et al. [16] analytically derived the stress field in and around a doubly periodic arrangement of TSVs subjected to a uniform thermal excursion. This model was extended to account for stress reductions caused by the onset of plasticity in the copper vias. The reliability of a TSV daisy chain under thermal cycling conditions was examined in Okoro et al. [17]. The electrical resistance was found to increase with the number of thermal cycles, due to thermally induced damage leading to the formation and growth of defects.

The conformality and electrical properties were evaluated on Al_2O_3 films deposited below 300 °C for through-silicon via (TSV) applications [18]. For the films deposited at 250 °C and 300 °C, the median breakdown fields with 30-nm-thick Al_2O_3 layer were above 6 MV/cm, they were inferior due to residual carbon impurities in the oxide layer. The dielectric via liner of through silicon vias was deposited at 400 °C, the thermal properties and electrical performance of blanket tetraethyl orthosilicate films were investigated by high temperature film stress and mercury probe capacitance - voltage measurements [19]. The TEOS SiO2 films show the advantages including good conformality, excellent densification, low thermal stress, high breakdown voltage and low current leakage. Fabricated TSVs are subjected to thermal cycling with temperatures ranging from −25 °C to 125 °C [20]. This study focused on thermal cycle testing of TSVs that had shown a high and electrically reliable yield in the DC tests. In the study of Krauss et al. [21], the thermal-dependent stress of thin tungsten films deposited either in full plate or on vias sidewalls were compared. The comparison of stress measurements at room temperature and during heating cycles reveals large differences between full plate and vias samples.

The failure criterion (or threshold) of a TSV structure under biased thermal stress have rarely been studied, and predictions of the earliest time and location of an element failure in these TSV components have also received little attention. The main point of this study is focused on the fracture model and numerical scheme developed for the solutions of the earliest element failure position and time arising in each component of the TSV structure and the corresponding strain energy density, $W_{failure}$. This numerical scheme is developed on the basis of the laboratory data of the TSV structure reported in the literature [10]. It shows the following works: (1) the parameters (coefficients) needed for the Johnson-Cook (J-C) model can be determined by conducting the microtensile tests per each component and using the software of genetic algorithm; (2) the earliest element failure or other physical process is predicted by the thermal strain that makes Ti and SiO_2 films and the Si wafer substrate to crack; (3) the critical stress and strain at potential failure locations are modeled by the use of the J-C constitutive model that allows the computation of local stress with an inclusion of stress relaxation by plastic flow; and (4) the strain rate effect can be coupled to the heating rate due to heat generated at Cu TSV; such approach is validated through the analysis on the failure location of the TSV. The $W_{failure}$ value per each component of the TSV is thus evaluated, and the effect of the joule heat in the Cu TSV on the $W_{failure}$ value is investigated. The thickness effects of the Ti and SiO_2 films on the maximum effective stress $\sigma_{\max}$ formed in the Si wafer are also examined.

2. The procedures to solve element failure solutions

In the present study, the experimental results of electrical current density and time to failure reported in the literature [10] are adopted as the reference data in order to validate the trustworthiness of the proposed numerical solutions. When using ANSYS/LS-DYNA software, the heat generation rate per unit volume of the Cu film and the heat flux passing through the bottom surface of the Si-wafer substrate in the TSV structure need to be evaluated and used as the two thermal/boundary conditions of temperature solutions, they are reliable only when the temperature and equivalent stress solutions predicted by the present models for the specific locations are close to those of the reported results [10]. By the stress and strain results and fracture strain data obtained from the microtensile tests, the fracture strain (ε^F) expressions for the Ti and SiO_2 films and the Si-wafer substrate are established through the uses of the Johnson-Cook fracture module in the software and the "Real-Coded Genetic Algorithm (RGA)" software. The "Steady-State Thermal: Temperature" module in the software is then applied to solve the temperature distributions in the TSV components. With the temperature solutions in the entire TSV structure, the steady element displacement and stress/strain vectors in all components of the TSV structure are then determined in sequence. These stress vectors are further applied to evaluate the mean stresses (pressures P_i, $i = 1,2,3\ldots$) acting on the annulus surfaces of the Cu TSV. The time-dependent P_i solutions are then served as the boundary conditions to solve the equivalent stress and strain distributions in the components of Ti and SiO_2 films and Si-wafer substrate. The numerical solutions of equivalent stress and strain in combination with these three ε^F expressions are provided to determine the element locations in the three TSV components (Ti, SiO_2 and Si) and the time of having the earliest failure. The solutions predicted by the present model are then checked to be trustworthy by the results of the current density varying with time shown in the reported literature [10]. The equivalent stress and strain corresponding to the earliest time of element failure in these three TSV components can be used to define the failure strain energy density ($W_{failure}$). The effects of element position and the rate of increase in the thermally-induced mean pressures (P_i, $i = 1,2,3\ldots$) on $W_{failure}$ are evaluated for these TSV components. The heat generation rates in the Cu film needed for $W_{failure}$ to occur in these three components are thus determined, and they can reveal the order in which the earliest failure will occur in these three components.

3. Details for microtensile tests to develop the Johnson-Cook Model for the component of TSV

The failure behavior arising in a TSV structure with complex geometries is very difficult to deal with using formal coordinate-based fracture