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Study of temperature-dependent charge conduction in silicon-nanocrystal/SiO_2 multilayers

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ABSTRACT

Silicon-nanocrystals (Si-NCs) realized by $SiO_{x<2}/SiO_2$ multilayer (ML) approach have shown promise for realizing tightly-controlled dimensions, thus efficiently exploiting the size-dependent quantum effects for device applications. Unfortunately, the confining insulating barriers (SiO_2 sublayers), instrumental for realizing quantum size effects in Si-NC MLs, can also hinder the charge conduction which is crucial for device applications including Si-NC based tandem solar cells and multi-exciton solar cells. Owing to this, a comprehensive study of conduction mechanisms has been carried out using a thorough analysis of temperature-dependent dark I-V measurements of SiO_2 thin film and Si-NC multilayer samples fabricated by Inductively Coupled Plasma CVD (ICPCVD). As the ML samples consisted of interleaved SiO_2 sublayers, current in SiO_2 thin film has initially been studied to understand the conduction properties of bulk ICPCVD SiO_2. For 21 nm thick SiO_2 film, conduction is observed to be dominated by Fowler–Nordheim (FN) tunneling for higher electric fields (>8 MV/cm; independent of temperature), while for lower electric fields (5–8 MV/cm) at higher temperatures, the trap-related Generalized Poole–Frenkel (GPF) is dominant. This signified the role of traps in modifying the conduction in bulk ICPCVD SiO_2 films. We then present the conduction in ML samples. For multilayer samples with SiO_2 sublayer thickness of 1.5 nm and 2.5 nm, Direct Tunneling (DT) is observed to be dominant, while for SiO_2 sublayer thickness of 3.5 nm, Space Charge Limited Conduction (SCLC) with exponential trap distribution is found to be the dominant conduction mechanism. This signifies the role of traps in modifying the conduction in Si-NC multilayer samples and SiO_2 sublayer thickness dependence.

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1. Introduction

Silicon at nanoscale dimensions (silicon nanocrystals; Si-NCs) is considered a potential material making use of quantum size effects. The superior properties of Si-NCs compared to bulk silicon include efficient light emission [1–7], quasi-direct bandgap behavior [8], size-tunable bandgap behavior [9], Stokes shift between emission and absorption [10–12], and multiple electron-hole pair generation per incident photon [13–19]. Si-NCs can thus be used for realizing various next generation devices including third generation photovoltaics [20–25]. It has been noted that the properties of Si-NCs are quite sensitive to the size of Si-NCs. Various approaches have been employed in the literature to realize tight size-controlled Si-NCs. Among other approaches, SiO_x/SiO_2 superlattice approach by Zacharias et al. [26] has the advantage of controlling the density of Si-NCs in addition to size by varying the stoichiometry (for density control) and thickness (for size control) of SiO_x sublayers. Various fabrication methods have been used to realize Si-NCs using this approach including magnetron sputtering [27], ion beam sputtering [28], thermal beam evaporation [26], electron-beam evaporation [10], low pressure CVD (LPCVD), hot wire CVD (HWCVD) and capacitively coupled plasma enhanced CVD (PECVD) [27]. In [29], we have shown inductively coupled plasma CVD (ICPCVD) as an excellent alternate fabrication method for realizing Si-NCs employing SiO_x/SiO_2 multilayer approach; ICPCVD uses high density inductively coupled plasma thus facilitating high quality thin film depositions at relatively lower deposition temperatures compared to other CVD methods. Owing to the encouraging results in realizing Si-NCs and further exploring the optical bandgap tunability reported in [29], this study focuses on electrical conduction study of Si-NC multilayers fabricated by ICPCVD.

Most of the existing literature in this area has focused on realizing Si-NCs using various approaches, verifying the crystallization and formation of Si-NCs during annealing and studying structural and optical properties of Si-NCs. A few attempts have been made to study the electrical properties of Si-NCs realized using SiO_2/SiO_x superlattice approach. Gutsch et al. [30] observed that, for SiO_2 sublayer thickness (T_{OX}) of 4 nm, the conduction resembles that of a 50 nm thick SiO_2 reference film, the conduction mechanism being Fowler–Nordheim (FN) tunneling for both the reference SiO_2 and ML sample. With the decrease

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in T_{OX} the coupling between the adjacent Si-NCs increases resulting in increase of current by orders of magnitude. This also indicates the change in conduction mechanism for varying T_{OX} values. Marconi et al. [31] observed Direct Tunneling (DT) with T_{OX} of about 3 nm for low fields while FN tunneling was observed for high fields. Rolver et al. [32] reported DT in Si/SiO_2 multilayers with T_{OX} of about 3 nm. The presence of traps also seems to affect the conduction mechanism in Si-NC ML samples. Gutsch et al. [30] observed Space Charge Limited Conduction (SCLC) for samples with 30 bilayers. Manousiadis et al. [33] studied lateral transport in Si-NCs employing Si/SiO_2 multilayers. For low voltages ohmic behavior was reported while for high voltages SCLC was reported. Lopez-Vidrier et al. [34] reported Poole–Frenkel (PF) conduction mechanism for SiON/SiO_2 superlattice with T_{OX} = 1 nm. Tao et al. [35] studied carrier transport in SiN_x/SiO_y Si-NC MLs, where PF was reported as the dominant conduction mechanism. It is noteworthy to mention that in these charge conduction studies, Si-NCs fabricated by PECVD [30–32,34], LPCVD [33] and Sputtering [35] methods were used. In this study we present, for the first time, a thorough analysis of temperature dependant charge conduction behavior of Si-NCs realized by ICPCVD employing SiO_2/SiO_x superlattice approach. It can also be noted that charge conduction mechanism in Si-NC MLs depends on several parameters including thickness of SiO_2 sublayer, number of multilayers, stoichiometry of SiO_x sublayer etc. Temperature dependence of various conduction mechanisms can be used to unambiguously arrive at the appropriate conduction mechanism [38].

Recently, we have reported fabrication of Si-NCs using ICPCVD and studied their structural [36,37] and optical properties [29]. In this work, a comprehensive study of conduction mechanisms was carried out by analyzing the temperature-dependent I-V measurements. We initially present the charge conduction in 21 nm thick SiO_2 film deposited by ICPCVD. We then present the analysis of temperature-dependent I-V of ML samples with SiO_2 barrier layer thickness varying from 1.5–3.5 nm for understanding charge conduction mechanisms in ML samples.

2. Experimental details

A 13.56 MHz ICPCVD system from Oxford Instruments (Plasma Lab System 100, ICP 180) was used for fabrication of four samples analyzed in this work: a SiO_2 thin film of 21 nm (# TF21 nm) and three ML samples (# 31ML-OX1.5 nm, # 31ML-OX2.5 nm, and # 31ML-OX3.5 nm). # 31ML-OX1.5 nm denotes ML sample with 31 multilayers of SiO_x/SiO_2 and nominal SiO_2 sublayer thickness of 1.5 nm. Each ML sample consisted of 15 SiO_2/SiO_x bilayer stacks and a final SiO_2 capping layer, giving altogether 31 MLs. Metal-Insulator-Semiconductor (MIS) structure was employed for all the samples for I-V characterization: Aluminum (Metal); Si-NC MLs or SiO_2 thin film (Insulator); 5 Ω − cm, p-type c-Si substrate (Semiconductor).

For SiO_2 deposition, the flow rates of SiH_4:N_2O:Ar gases were set to 7:20:10 sccm respectively whereas for SiO_x, the flow rates were set to 15:5:10 sccm respectively for all samples. All the samples were processed at a temperature of 250 °C, pressure of 4 mTorr with ICP power of 1000 W, and radio frequency (RF) power of 40 W. The stoichiometry of the SiO_x layer (i.e., x in SiO_x) with the same process conditions was estimated to be 0.8 using X-ray Photoelectron Spectroscopy characterization [29]. After deposition, all samples were annealed at 1100 °C in N_2 ambient; this critical processing step allows for crystallization and Si-NC formation in SiO_x sublayers. A detailed description of fabrication of the ML samples as well as TEM images, were reported earlier [29]. For # TF21 nm, a deposition time of 1 min resulted in thickness of 21 nm and refractive index of 1.46 as measured by ellipsometry. For all three ML samples, the deposition time of SiO_x sublayers is set constant at 30 s (4.6 nm nominal thickness [29]). An interface roughness of about 0.5 nm (about one or two atomic layers) on either side of SiO_x sublayer was observed in earlier studies [26,29]. This implies sublayer thickness variation of about ±0.5 nm. The three ML samples varied in the deposition time (and hence thickness) of SiO_2 sublayers: 7 s (1.5 nm nominal thickness) for # 31ML-OX1.5 nm, 12 s for # 31ML-OX2.5 nm and 17 s for # 31ML-OX3.5 nm [29].

Aluminum thermal evaporation was used to make both front and back metal contacts. A 200 nm thick circular Al dot of 1 mm diameter (made using shadow mask) was used as front contact. Thick (~200 nm) Al blanket deposition served as back contact. Upon making Al contacts, all samples were annealed in Forming Gas (FG) at 420 °C for 20 min to make good contact; this also results in hydrogenation of Si-NC MLs. The resulting structures used for electrical characterization are as shown in Fig. 1. The electrical I-V characterization was performed using Agilent B1500A semiconductor device analyzer with a thermal chuck by applying voltages on Al top contacts with respect to the back contact. The temperature dependent I-V measurements were carried out for all the samples by varying the chuck temperature from 25 °C to 200 °C.

3. Results and discussion

3.1. Conduction in SiO_2 thin film

As the ML samples consist of interleaved SiO_2 sublayers, understanding the bulk-limited conduction properties of SiO_2 thin film obtained by ICPCVD would be helpful in interpreting the conduction in ML samples. Accordingly, conduction in the SiO_2 thin film is discussed first. SiO_2 grown by thermal oxidation has been widely used in microelectronics and electrical conduction in such SiO_2 is well understood [38]. Thermal oxide is normally of high quality with less defects. Generally for thicker (5–50 nm) oxides, current conduction is explained by Fowler Nordheim tunneling while for ultra thin oxides (<3 nm) conduction is explained by Direct tunneling. Another widely used fabrication method for SiO_2 is chemical vapour deposition (CVD). CVD oxides generally tend to have more defects compared to thermal oxides. Conduction in thicker oxides with defects (like CVD oxides) is generally governed by Poole–Frenkel emission.

The voltage across SiO_2 thin film is corrected for work function difference (ϕ_{ms}) and band bending (ψ_s) in Si as described below. A p-type c-Si wafer with resistivity of 5 Ω-cm was used as starting substrate. This corresponds to doping density of about 3×10^{15} cm^{-3} assuming complete ionization [39]. The work function of the c-Si substrate is given by,

$$\phi_s = \chi + \frac{E_g}{2q} + kTln\left(\frac{N_a}{n_i}\right) = 4.1 + 0.56 + 0.31 = 4.97 \ \ V \quad (1)$$

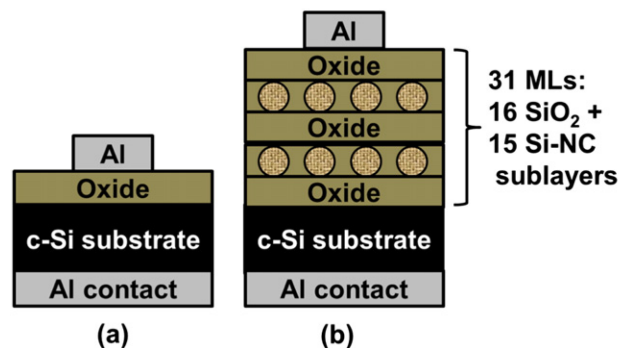

Fig. 1. Structures used for I-V analysis; (a) A SiO_2 thin film MOS structure, # TF21 nm. (b) ML samples employing Metal-Insulator-Semiconductor (MIS) structure: Aluminum (Metal); 31 Si-NC MLs (Insulator); 5 Ω − cm, p-type c-Si substrate (Semiconductor).

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