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Deep electron traps in HfO_2-based metal-oxide-semiconductor capacitors

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ABSTRACT

Hafnium oxide (HfO_2) is currently considered to be a good candidate to take part as a component in charge-trapping nonvolatile memories. In this work, the electric field and time dependences of the electron trapping/detrapping processes are studied through a constant capacitance voltage transient technique on metal-oxide-semiconductor capacitors with atomic layer deposited HfO_2 as insulating layer. A tunneling-based model is proposed to reproduce the experimental results, obtaining fair agreement between experiments and simulations. From the fitting procedure, a band of defects is identified, located in the first 1.7 nm from the Si/HfO_2 interface at an energy level $E_t = 1.59$ eV below the HfO_2 conduction band edge with density $N_t = 1.36 \times 10^{19}$ cm^{-3}. A simplified analytical version of the model is proposed in order to ease the fitting procedure for the low applied voltage case considered in this work.

1. Introduction

In recent years, much effort has been made in order to improve the program/erase performance and data retention of nonvolatile Flash memories beyond the 30 nm generation. The incorporation of high-κ dielectrics seems essential to this purpose. Particularly, hafnium oxide (HfO_2) was proposed as interpoly dielectric in replacement of SiO_2 in order to increase the control gate-floating–gate coupling ratio without reducing the oxide thickness, and thus avoiding the increase in leakage current [1–3].

Due to the stress-induced leakage current, cell-to-cell parasitic interference, and the need to wrap-around the floating-gate, the conventional floating-gate Flash memories would be replaced by charge-trapping nonvolatile memories [4], in which the charge is stored in discrete traps located inside a trapping layer. In this case, HfO_2 was proposed to replace SiO_2 as tunnel layer, which favors the charge injection due to the 1.5 eV electron tunneling barrier compared to the 3.2 eV in the case of SiO_2 [5]. HfO_2 was also considered to replace SiO_2 as blocking layer [5–7], ensuring an adequate capacitance value without reducing the oxide thickness. The combination of the two previous proposals results in the TaN/HfO_2/Ta_2O_5/HfO_2/Si structure [5]. However, since HfO_2 has an electron trap density many orders of magnitude higher than that of SiO_2 [8,9], the data retention could be seriously affected by low-field leakage current due to trap-assisted tunneling [10]. To solve this problem, a TaN/Al_2O_3/Ta_2O_5/HfO_2/Si structure was proposed, which has a better blocking efficiency due to the Al_2O_3 much larger barrier height [5].

HfO_2 was also proposed as trapping layer in charge-trapping memories as a replacement of conventional Si_3N_4, giving place to the metal/Al_2O_3/HfO_2/SiO_2/Si [11,12], showing a superior charge-storage capability at low voltages, faster programming, and less over-erase problems compared to conventional poly-Si/SiO_2/Si_3N_4/SiO_2/Si devices [13].

This paper contributes with experimental results through constant capacitance voltage transient (CCVT) measurements. This technique allows sensing deep traps and prevents the generation of new traps inside the dielectric. A physical model, previously developed for the study of electron traps in Al_2O_3 is used to get information on the energetic and spatial distributions of the deep electron traps inside the dielectric.

2. Experimental details

2.1. Samples description

Metal-oxide-semiconductor (MOS) capacitors with HfO_2 grown by atomic layer deposition (ALD) as insulating layer were studied. The samples were fabricated on an n-type silicon wafer with resistivity of

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1–12 Ω cm (phosphorous doping concentration of $4 \times 10^{14} - 5 \times 10^{15}$ at/cm^3). A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the HfO_2 ALD by photolitography and wet etching. Before deposition, the samples were first cleaned for 10 min with H_2O_2/H_2SO_4 followed by a 10 s dip in HF. The deposition equipment was a Cambridge NanoTech Savannah 200. The ALD process was performed at 225 °C and consisted in 100 ALD cycles, using tetrakis dimethylamido-hafnium (TDMAH) and water (H_2O) as precursors. Each ALD cycle was composed of a H_2O pulse of 30 ms, a N_2 purge for 6 s, a TDMAH pulse of 150 ms and a N_2 purge for 5 s. The process resulted in an oxide thickness of 10.5 nm, as measured by ellipsometry. Next, metalization with Al/(0.5%)Cu was performed. After patterning the metal layer by photolithography and wet etching, the back of the wafers was also metalized with aluminum for electrically contacting the silicon substrate. Finally, the wafers underwent a forming gas (N_2/(10%)H_2) annealing step at 350 °C for 20 min. The area of the obtained device was 3.24×10^{-4} cm^2. Fig. 1 shows a schematic cross-section of the fabricated device structure. The samples were characterized by transmission electron microscopy. The capacitance equivalent thickness of the HfO_2 layer was 3.4 nm [14]. A SiO_x interfacial layer (IL) was reported as a sub-product of ALD growth on Si [15]. We could not detect its presence through microscopy; we could neither exclude its presence.

2.2. Measurement technique and results

Successive cycles of capacitance–voltage (C–V) measurements at 1 MHz were performed with a computer controlled HP 4277A LCZ meter. Each C–V cycle consists of a first sweep from inversion at an applied bias (V_G) of −0.5 V to accumulation (V_G = 1 V) and back in the opposite direction. Fig. 2 shows the obtained curves along the first three cycles for a virgin device or after a sufficiently long (about 1 day) rest at room temperature.

The hysteresis is interpreted as electron capture in preexisting defects, also called hysteresis traps [16], inside the insulator during the sweep from inversion to accumulation, and the corresponding detrapping in the opposite direction. An interface states density of ~10^{12} cm^{-2} eV^{-1} was obtained through the stretch-out of the C–V curves.

The fact that the first sweep from inversion to accumulation differs from subsequent sweeps in the same direction implies that a fraction of electrons captured during the first C–V cycle are not discharged when the device reached the minimum voltage (V_G = −0.5 V), at the end of the sweep from accumulation to inversion. If the device is left unbiased for approximately 24 h, this fraction of electrons is detrapped and the subsequent sweep from inversion to accumulation results in the first cycle curve again. It is observed that while the accumulation to inversion C–V curve is the same regardless the number of C–V cycles performed, leading to the assumption that no new defects are generated during C–V cycles; the accumulation to inversion C–V curve

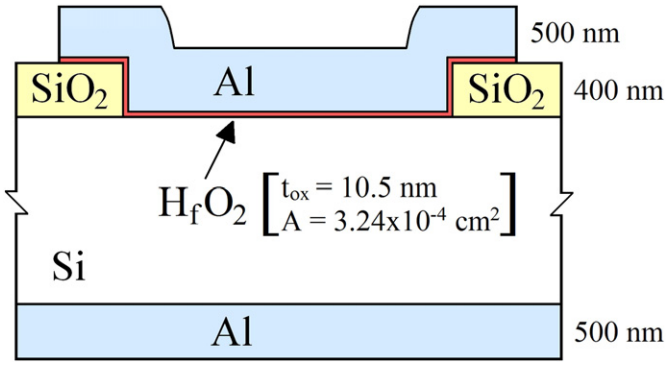

Fig. 1. Schematic cross-section of Al/HfO_2/Si stack.

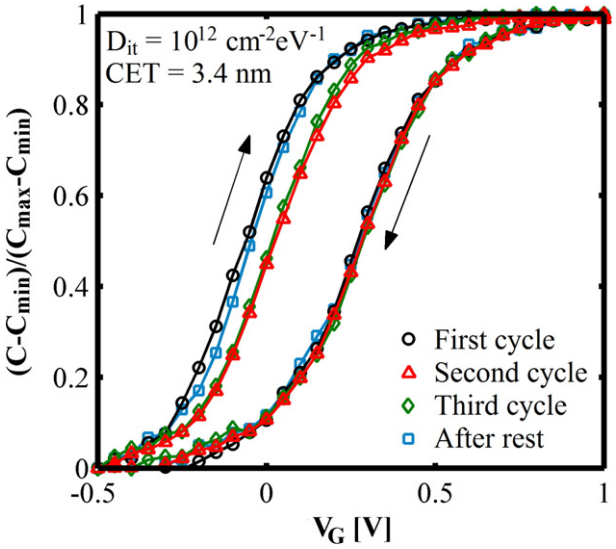

Fig. 2. Experimental first three C–V cycles for a virgin device or the corresponding one after a sufficiently long rest (one day at room temperature).

depends on the maximum voltage reached at the end of the inversion to accumulation sweep (Fig. 3), as reported by other groups [17,18]. This voltage dependence would be a consequence of an energetic distribution of electron traps, so that as bias increases, the Fermi level approaches the silicon conduction band edge, allowing for traps at higher energy levels to be filled by tunneling. Another possible explanation for this dependence is related to the fact that when the maximum voltage applied at accumulation increases, the sweep takes longer, which implies that tunneling affects traps far from the interface with the substrate. The latter possibility should be neglected for two reasons. First, the sweep time increases linearly with the maximum applied voltage, so that the hysteresis depends linearly with time. This dependence is not consistent with the usual log(t) dependence for the kinetics of tunneling processes (see Fig. 5 below). Moreover, from modeling (see Section 3), the discharges of traps filled during sweeps from different maximum applied voltages cover the same spatial region.

In order to gather information about the trapping/detrapping kinetics a complementary experiment was performed consisting of tracking the evolution of the voltage corresponding to a fixed capacitance (V_C)

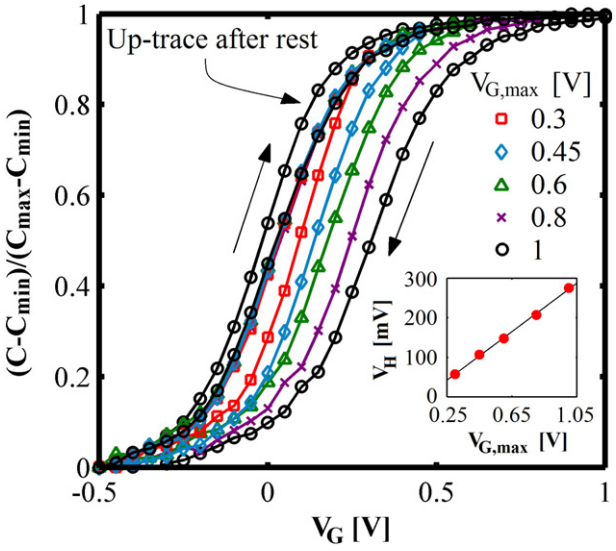

Fig. 3. C–V cycles with different maximum voltages $V_{G,max}$ at accumulation. It is observed that the hysteresis value V_H increases as $V_{G,max}$ increases, following a linear dependence as shown in the inset.