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Self-aligned double patterning process for subtractive Ge fin fabrication at 45-nm pitch

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ABSTRACT

The self-aligned double patterning scheme has been developed for subtractive Ge fin patterning targeting critical dimension (CD) < 14 nm at pitch of 45 nm. Compared to the Si self-aligned double patterning route, several modifications have been undertaken in different steps of Ge fin pattering, such as hard mask trimming and main etch. Out of several trimming options, it is the wet trim that has been qualified at the final stage of hard mask CD trimming. It allows meeting CD specifications for all structures and keeping straight lines without wiggling. Finally, the Ge main etch chemistry has been developed, which provides not only a straight fin profile but a flat etching front without depth loading attributed to different density structures.

1. Introduction

The effect of germanium channel introduction was shown [1] to be sizable up to the high performance expectations when technological nodes pass 10 nm. The performance boost offered by Ge channel for p-type fin-shaped field effect transistor (finFET) together with the possibility of n-type finFET fabrication makes it an attractive channel material to study.

The self-aligned double patterning (SADP) was selected to pattern Ge fins with 45-nm pitch (starting from initial 90-nm) and CD < 14 nm. In the Si SADP, it is the thickness of SiN spacer together with the final oxidation of the fins during shallow trench isolation (STI) oxide fill that determines the final fin's CD [2].

In contrast, the Ge fin fabrication does not rely upon extra trimming provided by oxidation component, that is why the CD of the hard mask (HM) should determine the final fin CD. The fact that in the Si SADP the typical CD after HM opening is ~20 nm means that in case of Ge fins the HM has to be substantially trimmed in order to get the right fin CD, which should be below 14 nm. Thus, the primary goal of the study was to reduce the CD of the lines patterned in the HM.

Another focus of the study was to develop the main etch step of Ge fin patterning at dense pitch. Even though the Ge fin fabrication has already been demonstrated for relaxed-pitch SiGe/Ge fins [3] and some of FET's electrical characteristics have been published [4,5], the first SADP experiments showed that the main etch chemistry has to be modified in order to meet the specifications (SPECs) of the 14-nm node structures.

2. Experimental

The dry plasma etch development was performed in the Lam Research 2300® Kiyo® E Series 300-mm conductor etch reactor. The $SiCl_4$-based advanced chamber condition control strategy was applied prior to etching of every individual wafer, which helps provide superior etch reproducibility [6].

Relaxed Ge substrates were fabricated by epitaxial growth of 1-μm Ge on standard Si(100) wafers that was followed by a chemical mechanical polishing (CMP) step targeting to remove the top 400 nm of Ge.

In this study we have performed the relaxed Ge fin pattering (CD < 14 nm), where the targeted depth of fin etch was set to be in the range of 120–140 nm. The final clean of the structure was performed ex situ in N_2O/forming gas plasmas followed by a short 0.6% HF clean [7].

Fig. 1 shows the patterning stack used for Ge fin SADP. It is composed of a standard combination of layers: resist, bottom antireflection coating (BARC), dielectric antireflection coating (DARC), advanced patterning film (APF), a-Si, SiO_2, and SiN. The SADP patterning steps are depicted in Fig. 2. The full SADP process includes three litho steps and four etching steps. Table 1 represents the SADP sequence used in the work, which is one of possible SADP patterning sequences often used in industry. The CDs obtained during the first transfer layer etching (called "CORE etch", shown in Fig. 2) determine the space target between fins in the final 45-nm pitch structure. However, CORE etch is not the only step that determines spaces between fins; each second space is determined by the SiN spacer deposition and its patterning. To perform the patterning in the final stage of SADP, the second transfer layer is used, see Fig. 1

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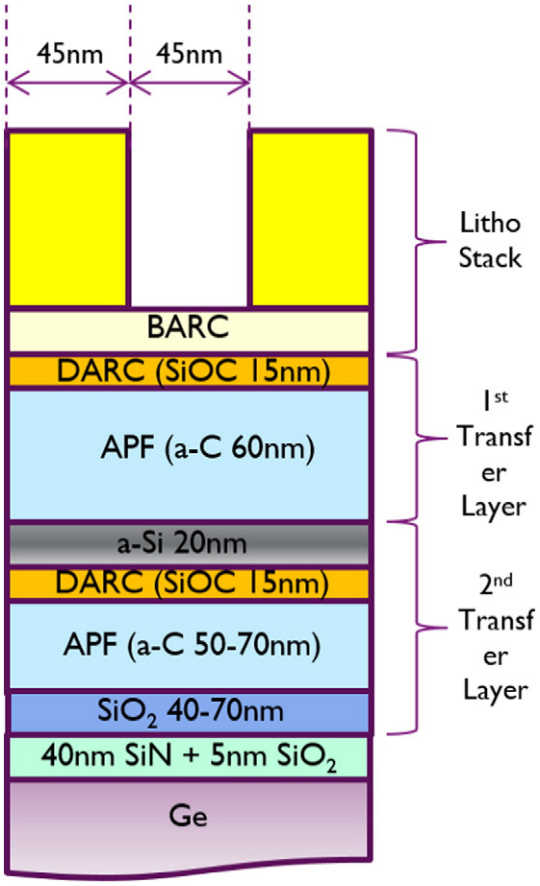

Fig. 1. The stack used for Ge fins SADP.

and Fig. 2. Thus, the thickness of SiN spacer deposited on top of the CORE structure determines not only the final fin's CD, but also each second space between fins.

3. Results and discussion

In SADP, the CD trimming can be done in different ways. The most straightforward approach is to deposit a thin spacer after CORE patterning, which thickness should define the CD of the lines in bottom SiN HM layer after the structure transfer. Thus, instead of putting the 40-nm SiN that is used in Si SADP flow, the SiN spacer thickness was reduced to 13 nm. In order to obtain an equal space between lines after SADP, the trimming time of CORE patterning has to be adjusted depending on the spacer thickness selected. For initial pitch of 90 nm and taking into account conformality of spacer deposition, one can write an empirical formula to estimate target CD at CORE depending on the thickness of spacer layer:

$$CD(nm) = (90 - \alpha * T_{SiN})/2,$$

where T_{SiN} is the thickness of SiN spacer layer, and α is a coefficient that is proportional to the conformality factor, so in our case it can roughly be taken as 1.

A corresponding trim time can be found from the linear fit of CD calibration curve for trimming times exceeding 10 s, see Fig. 3. Meanwhile, the dependence becomes non-linear when trimming time is short. The target CORE CD for the 13-nm SiN spacer test is close to 40 nm, so the CORE CD trimming was not performed.

Thus, the patterning of a thinner SiN spacer was demonstrated; however, the problem appears when the spacer-defined narrow lines have to be transferred into the bottom HM layers. It has been found that during the structure patterning either through the APF or through the SiO_2 HM layer, the narrow lines start to wiggle. The effect of wiggling is typically attributed to the stress level built up in a stack, which is relieved during its pattering. In the recent study of

Table 1
The SADP sequence used in the work. It is called "cut first" approach, when the cut is done before fin etching.

Step nr.	Step definition
1	Core litho
2	Core etch
3	Spacer deposition
4	Spacer etch
5	Core removal
6	Cut litho
7	Cut etch
8	Pad litho
9	HM opening and fin etch
10	Trench filling

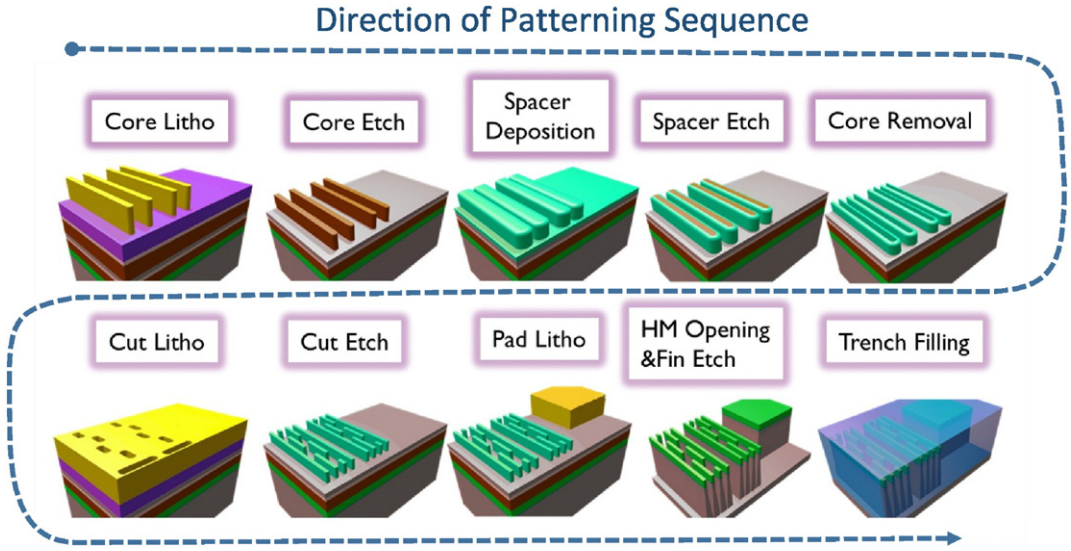

Fig. 2. Illustration of the steps used in the Ge SADP patterning scheme.