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Improvements in the reliability of a-InGaZnO thin-film transistors with triple stacked gate insulator in flexible electronics applications

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ABSTRACT

This study examined the impact of the low-temperature stacking gate insulator on the gate bias instability of a-InGaZnO thin film transistors in flexible electronics applications. Although the quality of SiN_x at low process/deposition temperature is better than that of SiO_x at similarly low process/deposition temperature, there is still a very large positive threshold voltage (V_{th}) shift of 9.4 V for devices with a single low-temperature SiN_x gate insulator under positive gate bias stress. However, a suitable oxide–nitride–oxide-stacked gate insulator exhibits a V_{th} shift of only 0.23 V. This improvement results from the larger band offset and suitable gate insulator thickness that can effectively suppress carrier trapping behavior.

1. Introduction

Recent portable electronic products have combined display [1–2], memory [3–5], and logic devices. Amorphous $InGaZnO_4$ (a-$IGZO_4$) material have attracted much attention due to their high mobility (>10 $cm^2/V\cdot s$), and low fabrication temperature, such as room temperature, which is suitable for the flexible display development. [1,6–13] However, for a-$IGZO_4$ thin film transistors (TFTs), because the traditional insulator deposition temperature via plasma-enhanced chemical vapor deposition (PECVD) at substrate temperatures of 350 °C is higher than the plastic substrate melting point of about 250 °C, the PECVD deposition temperature must be decreased in order to further develop flexible display applications. Furthermore, because the quality of SiN_x material at low process temperature is better than that of SiO_x material as shown in Fig. 1 and Fig. 2, the traditional SiO_x dielectric for gate insulator has been replaced by SiN_x. Moreover, comparing with the previous literatures, the gate dielectric quality at low deposition temperature is still poor enough to cause electric instability in the device [14]. Therefore, in this work, it shows that a triple-layer stacking gate insulator can effectively improve the stability under electric stress.

2. Experiment

In this study, the inverted-stagger structure a-$InGaZnO_4$ thin film transistors (TFTs) were fabricated on a glass substrate. After sputtering a 300 nm thick Ti/Al/Ti film deposition as gate electrodes, a single SiN_x or SiO_x gate insulator layer of about 300 nm was deposited using PECVD at 220 °C substrate temperature. As for triple-layer stacking gate insulators, the multi-dielectric structure of oxide–nitride–oxide (ONO) layers were deposited on gate electrodes. Furthermore, the front gate insulator thickness near the gate electrode was produced in three variations: 100, 300 and 500 A, while the total thickness of the gate insulator is fixed at 3000 A. The gate insulator thicknesses of the three types are 100/2600/300 A, 300/2400/300 A, and 500/2200/300 A, respectively. Next, a-$InGaZnO_4$ layers with thicknesses of 60 nm were deposited as channel layers by sputtering at room temperature for all of devices. A 200-nm-thick organic etching stop layer was deposited by spin coating. The source/drain electrodes were then formed by sputtering a 300-nm thick Ti/Al/Ti layer. And then 2 μm organic layer for passivation was deposited by spin coating. The channel width and channel length are 10 μm and 10 μm. These devices were operated under positive gate bias ($V_G = 30 + V_{th}$) and negative gate bias ($V_G = -30 + V_{th}$) for 1000 s, modified by initial threshold voltage (V_{th}) variation, while the source and drain were grounded. All measurements were made by an Agilent B1500 semiconductor parameter

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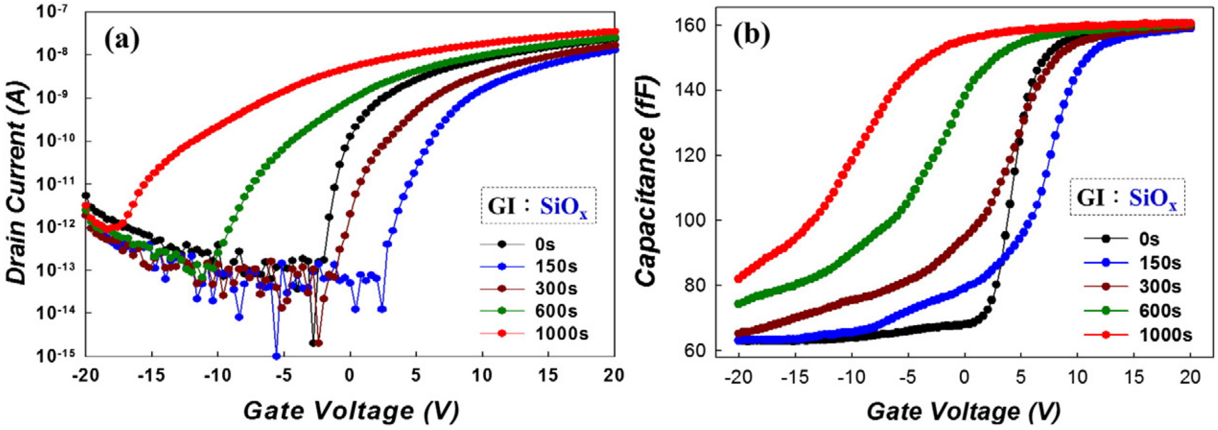

Fig. 1. The time evolution of (a) the transfer curves and (b) capacitance curve for a-IGZO TFTs with the single SiO_x gate dielectrics as a function of the applied positive bias stress time.

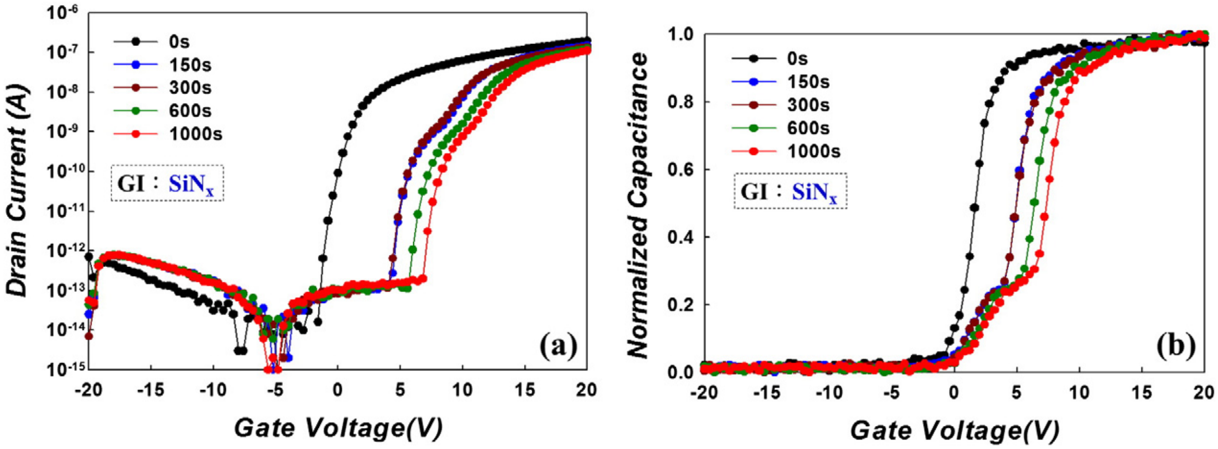

Fig. 2. The time evolution of (a) the transfer curves and (b) capacitance curve for a-IGZO TFTs with the single SiN_X gate dielectrics as a function of the applied positive bias stress time.

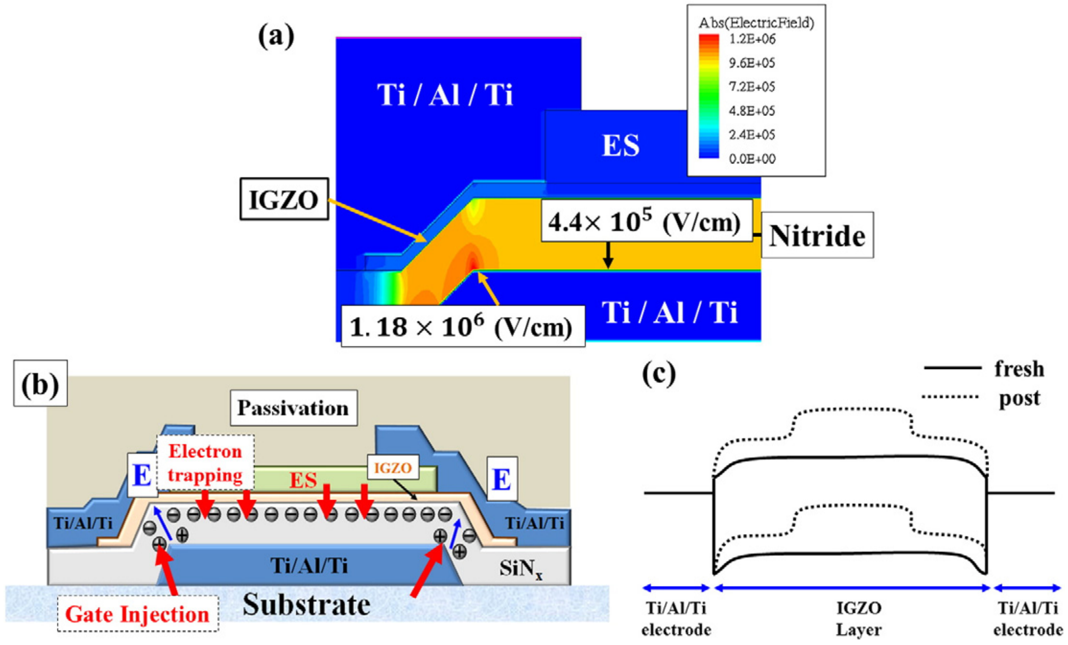

Fig. 3. (a) The electric field distribution of schematic cross section for ISE-TCAD simulation. (b) Schematic cross section of a-$InGaZnO_4$ structure. (c) The energy band diagram horizontal to the channel direction.