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Subthreshold slope as a measure of interfacial trap density in pentacene films

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ABSTRACT

Electrical properties in organic field effect transistors (FETs) are dominated by charge transport in the accumulation layer, few molecular layers close to the gate dielectric. Through comparison of the subthreshold slope between monolayer (ML) and thick pentacene FETs, formation of the second layer islands on top of the complete first layer is found to be crucial in determining the charge transport in ML pentacene FETs. It is demonstrated that a pentacene ML field effect transistor (FET) is an excellent probe that can detect electronic states of organic semiconductors interfacing with the gate dielectric at nanometer scale. Far higher sub-threshold slope in ML FETs, as a measure of interfacial charge trap density, than that in thick pentacene FETs is translated that the path of the induced carriers in ML FETs is limited into the molecular layer interfacing with the gate dielectric with a high density of charge traps, while carriers in thicker films have alternative pathways through more electrically conductive layer above the first layer with much less trap density.

1. Introduction

Monolayer (ML) organic field effect transistors (FETs) have been researched due to the length scale of the accumulation layer set by the effective Debye length [1–7]. In organic FETs, organic semiconducting layer close to the gate dielectric, away from less than 1 nm, is the region where most of the charge carriers are induced [8–10]. Therefore, it has been predicted that charge transport in ML-thick organic semiconducting layers between source and drain electrodes dominates the electrical performance of the FET device as long as the thickness of the active layer is larger than the effective Debye length [11,12].

Unlike the theoretical prediction, however, a number of studies showed that the theoretical accumulation layer thickness was not consistent with the effective Debye length beyond which no significant charge transport occurs [5,13,14]. Many groups have reported thickness dependence of FET device performance using in-situ electrical measurements for small molecular weight organic semiconductors [13,14]. Mobility and threshold voltage have been monitored as a function of thickness through in-situ electrical measurements [14]. In the study, the saturation thickness of mobility was different sample to sample and the threshold voltage shift to a more positive value was observed during pentacene growth. In many studies, delay of saturation has been attributed to a number of reasons including the presence of traps at the interface, traps in the organic materials, and morphology depending on growth mode [13–16]. Furthermore, it has been reported that carrier transport in ML-thick FETs was quite different from that in thick organic semiconducting films. Large hysteresis accompanied with a large negative threshold voltage and high metal-semiconductor contact resistance were observed in ML transistors [5,14].

Despite a number of studies of the accumulation layer, however, study of the origin of the difference between ML and thick organic semiconducting FETs still lags behind because, in many of the studies, fabricating FETs with optimum thickness has been more highlighted rather than understanding the high sensitivity of a ML FET arrangement to the interface-induced organic semiconducting layer. In typical current voltage characteristic measurements for ML FETs, the contribution of a single organic semiconducting ML interfacing with the gate dielectric to the total current is maximized. It is surprising that, in other words, ML FETs as sensitive probes of the organic semiconducting layer at functional interfaces have not been focused. Further, difference in the subthreshold slope between ML and thick film FETs, as a measure of interfacial and (or) bulk charge trap density, has not been emphasized [17–19]. Exploring the origin of difference in the subthreshold slope can provide insights into not only understanding electronic properties of organic semiconducting materials in contact with functional interfaces, crucial in driving flexible electronic devices including organic light emitting diodes (OLEDs) and organic photovoltaics (OPVs), but also tracking the path of the carriers induced in the organic semiconducting layer interfacing with the gate dielectric.

In this Letter, interfacial and bulk trap density in a pentacene ML FET were estimated through analysis of the subthreshold slope and the discrepancy in the trap density between ML and thick films is explained by the path of the induced carriers. Pentacene was used as an active layer because its well defined layer by layer growth mode on SiO_2 is well suited to correlate morphology to charge transport at nanoscale.

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The magnitude of the trap density in a ML FET including the interface charge traps and the bulk traps was compared with that of a thick pentacene FET, emphasizing the ML FET as a probe of interface-induced charge trap density in organic semiconducting layers.

2. Experimental methods

A bottom-contact FET was structured to measure the electrical properties of the accumulation layer close to the SiO_2 interface. The source and drain electrodes [Au (60 nm)/Cr (3 nm)] were photolithographically patterned onto a 200 nm SiO_2 gate dielectric. Highly doped silicon substrate served as a gate electrode. Pentacene molecules were deposited using thermal evaporation at a vacuum chamber at a working pressure of 10^{-7} Torr. The deposition rate was varied between 0.01 and 0.3 Å/s. The in-situ electrical measurements were carried out in vacuum through electrical feedthroughs wired to FET devices without exposure to air. To probe the morphology of pentacene films at thicknesses ranging between submonolayer and ~50 nm, tapping mode atomic force microscopy (AFM) was used, enabling estimation of deposition rate by dividing the area coverage of pentacene by deposition time. It is noted that the coverage of 1 ML is equivalent to a complete layer with a uniform thickness of a single molecular layer that covers the entire area between the source and drain electrodes.

3. Results and discussion

Charge transport properties of the carriers induced at a pentacene molecular layer in contact with the gate dielectric were measured in a vacuum chamber without the effect of air degradation that creates carrier trap sites. The experimental setup for in-situ electrical measurements is shown in Fig. 1(a). At a coverage of 0.93 ML in Fig. 1(b), pentacene islands (bright colored) on the SiO_2 gate dielectric (dark colored) were coalesced, producing the conduction pathways for transport of holes. The height of the first pentacene ML was ~1.6 nm consistent with the molecular length of a pentacene molecule [20–22]. Transport of holes induced by the gate electric field is confirmed in the output transistor characteristic curves in Fig. 1(c). In the linear regime in transistor operation [11], the magnitude of the drain voltage, V_D, is far smaller than the gate voltage, achieving uniform carrier concentration in the channel between the source and drain electrodes. The magnitude

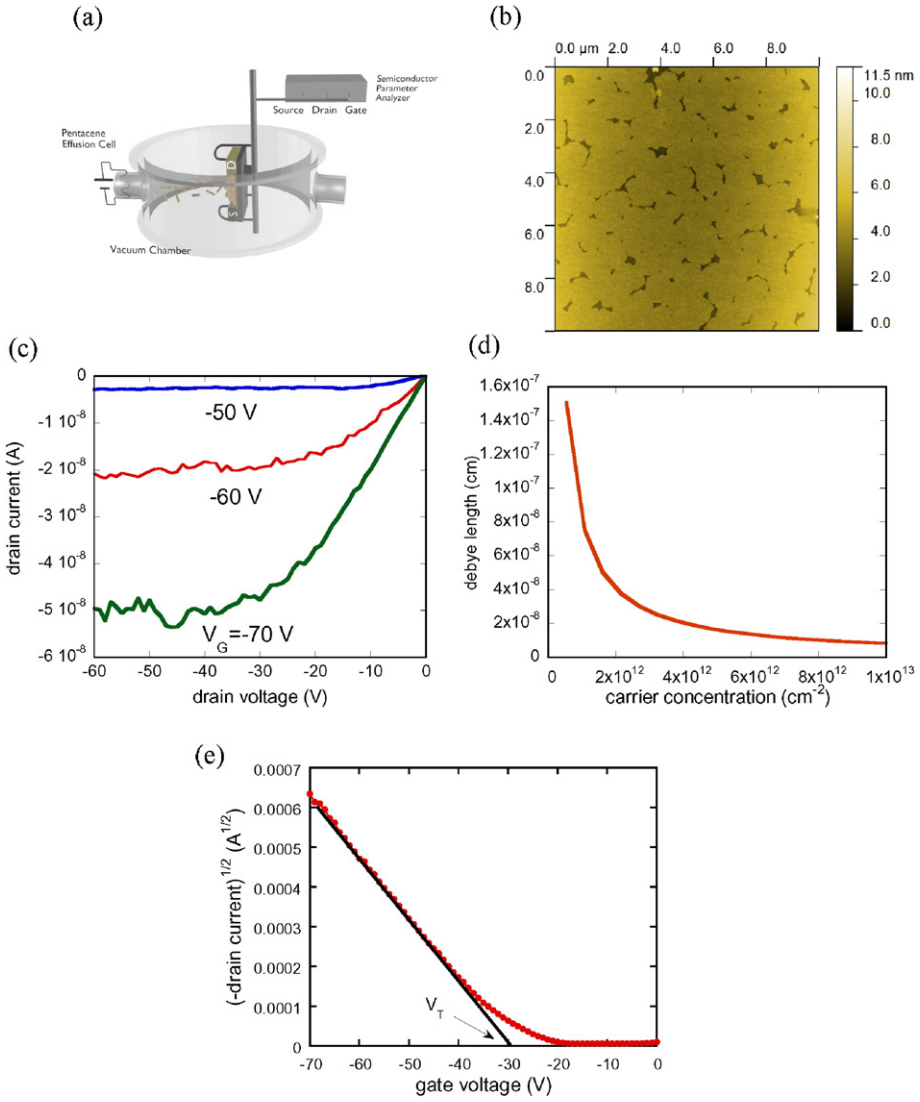

Fig. 1. Electrical setup for in-situ measurements during pentacene growth. The deposition rate is controlled by varying the temperature of the effusion cell through resistive heating. (b) AFM image of a sub-monolayer (0.93 ML) pentacene film grown at a deposition rate of 0.01 Å/s. (c) I_D–V_D characteristic curves for the ML pentacene FET. The channel length and width are 40 μm and 1 mm, respectively. (d) Debye length as a function of carrier concentration. (e) $I_D^{1/2}$–V_G plot at the saturation transport regime. The FET mobility was 1.1×10^{-3} cm^2/Vs and the drain voltage was fixed at −50 V.