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Quantification of sputtering damage during NiO film deposition on a Si/SiO_2 substrate using electrochemical impedance spectroscopy

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ABSTRACT

Sputtering damage during NiO deposition on SiO_2 coated Si^+ substrate is investigated using an electrochemical impedance spectroscopy. The degree of sputtering damage for samples located at different positions relative to the sputtering source is evaluated by proposing an equivalent circuit that includes a constant phase element (CPE) to represent the area around the SiO_2/NiO interface. By fitting the impedance data, CPE-T and CPE-p index parameters (which are related to the interface uniformity and quality) are obtained. Using these parameters, the capacitance and time constants of the SiO_2 layer and the SiO_2/NiO interface are estimated. By comparing the CPE-p index values, it is concluded that the sample that is closer to the sputtering target is exposed to more damage than samples located at greater distances during the deposition process. This result is significant because it may help to reduce growth-related defects and improve the quality of NiO films grown using the sputtering technique.

1. Introduction

Recently, oxide-based transparent semiconductors have attracted the attention of many researchers because of their potential application in optoelectronic devices and transparent electronics, such as flat-panel displays, detectors, solar cells, active-matrix display elements, and thin-film transistors [1–7]. Among these semiconductors, nickel oxide (NiO) shows p-type conductivity [8–10] and is a suitable material for forming a pn-junction with other n-type oxide semiconductors, such as indium tin oxide (ITO), indium zinc oxide (IZO), and zinc oxide (ZnO). With its 3.7-eV band-gap energy, NiO absorbs only UV light, which is harmful to humans; therefore, NiO is suitable for use in the fabrication of transparent semiconductor devices. In addition, NiO is safe to handle and is made using environmentally friendly and inexpensive materials, unlike semiconductors comprised of other compounds. Although NiO offers many advantages, the growth of high-quality p-type NiO remains a challenging task. Compared with other methods, such as pulsed laser deposition, oxidation of Ni, and chemical deposition, the growth of large-area NiO thin films using the sputtering technique is convenient, inexpensive, and relatively simple [7,11–13]. However, the sputtering technique remains somewhat problematic because of the energetic charged particles used during the deposition process. Bombarding the substrate with energetic ions introduces some defects, which are undesirable, especially for optoelectronic devices. However, sputtering damage is difficult to estimate using conventional and nondestructive methods. Because sputtering is suitable for large-scale mass production, finding nondestructive methods to estimate growth-related damage is an important endeavor.

Electrochemical impedance spectroscopy (EIS), which has been used extensively in chemical material research [14–16], is becoming more popular as an analytical tool for investigating complex semiconductor device structures, including pn-junctions and new-generation solar cells, like $Cu(In,Ga)Se_2$(CIGS)-related solar cells [17–23]. Compared with other conventional techniques (such as capacitance measurement, admittance spectroscopy, and deep-level transient spectroscopy), the advantage of EIS is that it provides more comprehensive data to estimate both the capacitance value of the complex stacked layers and the quality and uniformity of the interfaces. Recently, this technique has been applied to estimate the uniformity of the CdS buffer layer and the sputtering damage resulting during n-type layer deposition in CIGS solar cells [17,18], which are issues that are difficult to investigate using other techniques.

In this study, the EIS technique is utilized to quantitatively estimate sputtering damage. For this purpose, unintentionally doped NiO films are deposited on a Si^+/SiO_2 substrate and are analyzed to estimate the influence of sputtering damage near the SiO_2/NiO interface. Based on our results, both the application of the EIS technique to the estimation of sputtering damage and the possibility of finding a correlation between EIS data and the sputtering configuration are discussed.

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2. Experimental detail

To investigate sputtering damage during NiO deposition, a 200-nm-thick NiO layer is deposited using reactive RF magnetron sputtering on identical substrates that are located at different positions relative to the target. To simply and restrictively consider EIS analysis, a commercially available high-quality Si^+/SiO_2 substrate is chosen to ensure that the quasi-ideal Si^+/SiO_2 is not responsible for a significant contribution to the EIS signal. All NiO films in this study are deposited on a 100-nm SiO_2 layer on 400-μm n-type (100) Si^+ substrate that has resistivity $\rho_{Si} \leq 0.018$ Ωcm, as shown in Fig. 1(a). The unintentionally doped NiO layer shows p-type conductivity with a carrier concentration of about 10^{15} cm^{-3}. The substrates are characterized as the top, side, and wall, depending on their relative position and the distance (d) between the substrate and the sputtering target; the distances are $d_{top} = 17.0$ cm, $d_{side} = 21.2$ cm, and $d_{wall} = 24.5$ cm, respectively, as shown in Fig. 1(b). For the present experiments, NiO sputtering deposition is conducted with unintentional heating at 3.9 Pa with Ar and O_2 serving as the sputtering and reactive gases, respectively. The O_2 fraction in the sputtering gas $[O_2/(Ar + O_2)]$ is 0.5%, and the RF power is set at 150 W.

The impedance measurement is conducted using an NF FRA5087 frequency response analyzer with frequencies ranging from 0.1 Hz to 10 MHz. To change the band bending and/or interface properties, a 1.0-V AC signal is applied to the samples. For bias-voltage-dependent measurements, a DC bias voltage is applied to the sample from the analyzer's internal DC power supply. For that condition, positive bias is defined when Si^+ is positively polarized and NiO is negatively polarized; negative bias is the converse. All measurements are taken at room temperature and in dark conditions. After measurement, Z-plot software is used to fit the impedance data to obtain the acquired parameters.

3. Results and discussion

Typical impedance spectra (IS), called Nyquist plots, of the top sample are shown in Fig. 2(a) as a function of the applied DC bias voltages. In addition, the enlarged IS of the high-frequency region is shown in Fig. 2(b). In these graphs, the horizontal axis and the vertical axis show the real (resistive) and imaginary (capacitive) part, respectively, of the impedance (Z); the frequency parameter increases as the resistance decreases on the real axis. The IS shown in Fig. 2 always has double semicircles, regardless of bias voltage, and one of these semicircles always appears in the high-frequency (~10^6 Hz) region, while the other frequency is present in the low-frequency (~10^3 Hz) region, even though the relative radius changes with the bias voltage. This result indicates the existence of two different combinations of resistive

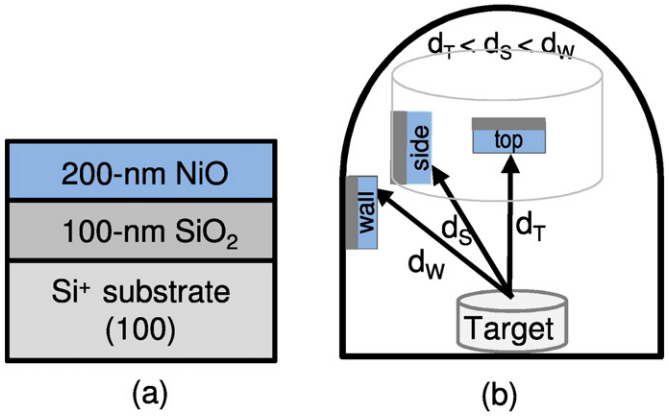

Fig. 1. (a) Layer structure and (b) position of the samples in the chamber during the growth process.

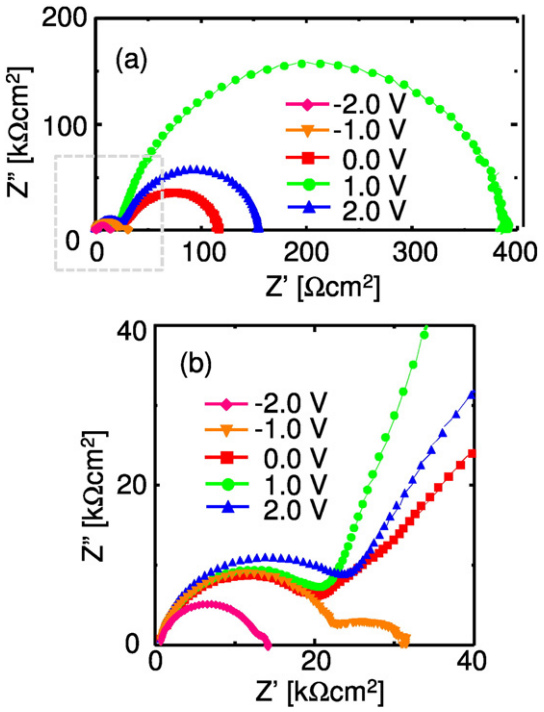

Fig. 2. Bias-voltage dependence of the IS for (a) the top sample in full scale and (b) the magnified portion in the high-frequency region.

(R) and capacitive (C) elements in the $Si^+/SiO_2/NiO$ interfaces. The variation in the semicircles' radii depends on the applied bias voltage, and this relationship is significant and relates to the electrical properties of the corresponding interface. The semicircle structure at low frequency depends strongly on the applied bias. Conversely, the structure of semicircle at high frequency does not change significantly with the applied bias voltage. Another interesting feature of the IS in relation to the bias voltage is that, when the positive bias voltage is further increased, the radius of the semicircle at the low-frequency end starts to decrease beyond a certain (turnover) bias voltage. From the bias-dependent measurement, the turnover voltage is estimated to be about +1.0 V and is approximately the same for all three samples. The IS has a similar dependence on the applied bias voltage. For example, the double semicircle (the variation in the relative radius with respect to the bias voltage and the turnover voltage) is observed for all samples. We discuss this mechanism later.

To evaluate the sputtering damage around the $Si^+/SiO_2/NiO$ interfaces using the EIS technique, it is necessary to identify the contributions to the IS signal that originate from several layers/interfaces separately. We define the equivalent circuit of the CIGS thin-film solar cell structure to account for several interfaces [17,18]. Because there are two semicircles in the IS graph in this case, it is natural to assume that the main contribution results from only two layer/interfaces, which are around the Si^+/SiO_2 interface and around the SiO_2/NiO interface. Based on the experimental IS data, some of these possibilities can be excluded, and the source of the signal can be pinpointed. Because the Si^+/SiO_2 substrate is an industrial quality standard, the interface's effect (such as its defects and/or inhomogeneity) is neglected. However, the area around the SiO_2/NiO interface is not ideal because it contains defects and/or inhomogeneity resulting from sputtering damage. A proposed equivalent circuit is shown in Fig. 3 with an appropriate Nyquist plot. This circuit consists of a series bulk resistance (R_{bulk}), a capacitance ($C_{Si+/SiO2}$), and a capacitance-like element (a constant phase element [CPE]) in addition to a parallel resistance, given by $R_{Si+/SiO2}$ and $R_{SiO2/NiO}$, which represent the Si^+/SiO_2 and SiO_2/NiO layers, respectively. A CPE element has an impedance response that displays non-ideal frequency-dependent properties and a constant phase over the