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Monolayer field effect transistor as a probe of electronic defects in organic semiconducting layers at organic/inorganic hetero-junction interface

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ABSTRACT

The origin of a large negative threshold voltage observed in monolayer (ML) field effect transistors (FETs) is explored using *in-situ* electrical measurements through confining the thickness of an active layer to the accumulation layer thickness. Using ML pentacene FETs combined with gated multiple-terminal devices and atomic force microscopy, the effect of electronic and structural evolution of a ML pentacene film on the threshold voltage in an FET, proportional to the density of deep traps, was probed, revealing that a large negative threshold voltage found in ML FETs results from the pentacene/SiO_2 and pentacene/metal interfaces. More importantly, the origin of the threshold voltage difference between ML and thick FETs is addressed through a model in which the effective charge transport layer is transitioned from the pentacene layer interfacing with the SiO_2 gate dielectric to the upper layers with pentacene thickness increasing evidenced by pentacene coverage dependent threshold voltage measurements.

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1. Introduction

Organic semiconducting materials (OSMs) [1–3] have attracted much interest because they can be incorporated into flexible electronic devices including organic field effect transistors (OFETs) [4,5], organic light emitting diodes (OLEDs) [6–8] and organic solar cells (OSCs) [9–11]. OSMs in the devices are required to possess high carrier mobility and low operating voltage for decent device performance. Considering charge carrier transport in the π-electronic system governs the main features of the organic electronic devices, intermolecular interactions and the degree of structural order are the key issues to address. Particularly, charge transfer and transport in OSMs are often limited by defects associated with the two factors, requiring understanding of electronic trap states in OSMs [12].

The presence of localized electronic states within OSMs has been reported to be critical in determining device operation thereby device efficiency because charge transfer/transport in OSMs is significantly affected by the nature of localized states [13,14]. In OLEDs, for example, electrons and holes are injected through the anode and cathode electrodes, and recombine in the emission layer. The luminous efficiency is determined by the loss in active layers before carrier recombination [15]. In OSCs, charge trapping and recombination following exciton dissociation at an electron donor/acceptor interface [11,16] are important issues in determining the open circuit voltage and short circuit current [17–19].

It is important to focus on the molecular interactions and structural disorder at the nanometer scale because the length scale associated with charge transfer and transport at organic electronic devices is comparable to few molecular layers [3,17]. In OFETs, for example, the accumulation layer, characterized by Debye length is a few *nanometer*. In OSCs, the exciton diffusion length is less than 10 nm [11,20]. Moreover, as the dimension of the devices becomes nanosized and component materials are hybridized for interfacial functionalization, understanding electronic states at the hetero-junction interface is crucial. In other words, electronic localized states at the nanometer scale should be separately explored from the bulk.

OFETs provide a versatile platform to explore the electrical properties of OSMs at a nanometer scale because the current–voltage characteristics are dominated by the two-dimensional (2D) carrier confined sheet (accumulation layer) close to the gate dielectric [21–23]. As variables for the current–voltage characteristics, the threshold voltage and the FET mobility are key parameters in correlating the electronic properties of the localized states to the structural properties of OSMs [22]. Particularly, the magnitude of the threshold voltage, the gate voltage required to induce mobile carriers in the electrical channel, has been linked to the concentration of electronic traps, providing insights into electronic defects in OSMs embedded in organic electronic devices. The FET mobility can be translated into the carrier transport efficiency from which structural ordering and electronic localized states can be explored.

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Understanding the origin of the electronic trap states in OSMs interfacing with other materials is one of the main issues in optimizing and controlling device parameters of flexible electronic devices [24,25]. Study of the origin of threshold voltage has been carried out through a number of literatures [26–35]. In the study, the magnitude of the threshold voltage has been tuned through various strategies including surface treatment of the gate dielectric or introduction of a layer with interface dipole, concluding that the threshold voltage is largely determined by the gate dielectric/organic semiconductor interface. However, most of the studies have focused on the thick organic semiconducting films, neglecting change in the structural and electrostatic properties with thickness increase within the effective charge transport thickness (Debye length). Fiebig et al. [26] in which threshold voltage was monitored up to a thickness of ~40 nm claims that threshold voltage change with thickness is attributed to increase in the volume traps with thickness increase. However, it still fails to provide a comprehensive understanding associated with subtle change of intrinsic properties of the active layer separate from the contact effects within the accumulation layer regime.

Confining the probing area to a few nanometers by electro-gating using the FET structure allows for exploring the origin of deep traps systematically. In the perspective, FETs incorporating monolayer (ML)-thick active layers (ML FETs) are desirable for the study due to the length scale of the effective charge transport. Particularly, pentacene is a representative low molecular weight organic semiconducting material with a high FET mobility. Pentacene FETs assembled onto the SiO_2 gate dielectric surface are well suited for interface study because pentacene molecules form a ML with a uniform height on the SiO_2 surface, allowing for correlation between electronic and structural properties [36]. In this report, a comprehensive study of the origin of the large threshold voltage in ML pentacene FET devices is carried out through *in-situ* electrical measurements in which pentacene coverage is controlled at a nanometer scale in combination with atomic force microscopy (AFM). Threshold voltage change with a subtle structural change within the accumulation layer thickness is monitored and correlated to the transition of the effective charge transport layer from the pentacene ML in contact with the gate dielectric to the upper layer. The effect of the contact resistance on the threshold voltage is clarified within the accumulation layer thickness.

2. Experimental section

Pentacene was purchased from Sigma Co. and was thermally evaporated at a vacuum chamber at a pressure of 10^{-7} Torr. The deposition rate was varied between 0.04 and 6 nm/min. FET devices were fabricated from a conventional photolithography in which source and drain electrodes were patterned onto a 200 nm-thick SiO_2 gate dielectric. Highly doped silicon substrate served as a gate electrode. Prior to pentacene deposition, bare FET devices were ozone-cleaned, followed by sonication in acetone, methanol and deionized water. Pentacene was pre-evaporated for hours before deposition. In the *in-situ* measurements, gate voltage was scanned between −50 and −80 V periodically at a constant drain voltage of −50 V during pentacene growth. A shadow metal mask was used to confine the active area in which pentacene is deposited to the channel region between the source and drain electrodes. Deposition rate of pentacene was estimated in a submonolayer coverage in which pentacene islands with a height corresponding to a molecular length of ~1.5 nm [37] covers the SiO_2 substrate. To calculate the deposition rate, the area covered by pentacene islands, calculated from the *ex-situ* AFM images of pentacene films, is divided by the deposition time. Temperature dependent charge transport measurements were carried out in a vacuum chamber equipped with a cryostat. All the electrical measurements were carried out in vacuum without exposing to air excluding complications arising from adsorption of water and oxygen.

3. Results and discussion

Threshold voltage is the gate voltage required to induce mobile carriers in the electrical channel between source and drain electrodes. In probing the electrical properties of OSMs using FETs, threshold voltage has been interpreted as a measure of deep traps. According to Podzorov et al. [38], charge carriers in OSMs close to the gate dielectric, induced by the gate electric field preferentially fill the deep traps lying a few k_BT (~0.1 eV) away from the highest occupied molecular orbital (HOMO), positioning the Fermi energy level closer to the energy level of the shallow traps. Filling the deep traps, the number of mobile carriers induced by the gate-field increases dramatically, achieving a threshold voltage.

Threshold voltage in a pentacene FET can be extracted from the linear or saturation transport regimes by calculating the gate voltage at which the drain current is zero from the region in which the drain current changes linearly with the gate voltage in the drain current (I_D) *vs.* gate voltage (V_G) curves (linear region) or $I_D^{1/2}$ *vs.* V_G (saturation region) curves, respectively. As shown in I_D–V_G curve of Fig. 1(a), threshold voltage is calculated from extrapolation in the transport region in which the drain current linearly increases with gate voltage. It is noted that, during gate voltage scan in a low gate voltage region, induced carriers by the gate voltage fill the deep traps preferentially resulting in a gradual increase in I_D with increasing V_G. The resulting curvature the I_D–V_G curve disappears at the high gate voltage region with the I_D–V_G curve becoming linear, allowing for determination of the threshold voltage. This clearly indicates that, as the negative gate voltage increases, the mobile carriers dominate charge transport properties. In this paper, the threshold voltage and mobility values were obtained at a high gate voltage region to minimize the effect of the carrier trap sites on charge transport. For thick films, the threshold voltage was extracted in the gate voltage region between −20 and −50 V, while for ML films it was extracted in a higher gate voltage region between −40 and −60 V, reflecting a large negative threshold voltage in ML FETs. The pentacene film thickness was ~100 nm corresponding to about 67 pentacene molecular layers. In the linear regime in transistor operation, the drain voltage, V_D, is far smaller than the gate voltage, satisfying an almost uniform charge carrier concentration independent of the position between the source and drain electrodes. The FET hole mobility, μ, and the threshold voltage, V_T, are given by Eq. (1);

$$I_D = \frac{Z}{L}\mu C_{ox}(V_G - V_T)V_D \tag{1}$$

where C_{ox} is the capacitance of the gate dielectric, and Z and L represent the channel width and length, respectively. The number of hole carriers induced by a negative gate voltage linearly increases at a small drain voltage (linear regime) followed by saturation at a high drain voltage ($V_D = V_G - V_T$) because the depletion region becomes wider with the drain voltage increasing as given by Eq. (2) representing the saturation regime as seen in Fig. 1(b).

$$I_{D,sat} = \frac{Z}{2L}\mu C_{ox}(V_G - V_T)^2 \tag{2}$$

As shown in Fig. 1(a), the threshold voltage in thick pentacene FETs is close to zero, consistent with a number of previous reports [39]. At a given threshold voltage, the density of states for the deep traps can be estimated using temperature dependent I_D–V_G measurements in Fig. 1(a). The FET mobility, proportional to the slope of the I_D–V_G plots, decreased with decreasing temperature, consistent with thermally activated hole transport [4,40]. More importantly, as temperature decreases the threshold voltage decreased linearly in Fig. 1(c). The linear dependence of the threshold voltage with temperature indicates that the density of deep traps is independent of energy based on the relation, $\delta N_{tr} / \delta E = (C_{ox} / k_B e)(\delta V_T / \delta T) = 1.1 \times 10^{11}$ cm^{-2} eV^{-1}, proposing the energy band diagram shown in the inset of Fig. 1(c). The presence of a

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