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Study on the graphene/silicon Schottky diodes by transferring graphene transparent electrodes on silicon

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ABSTRACT

Graphene/silicon heterostructures present a Schottky characteristic and have potential applications for solar cells and photodetectors. Here, we fabricated graphene/silicon heterostructures by using chemical vapor deposition derived graphene and n-type silicon, and studied the electronic and optoelectronic properties through varying their interface and silicon resistivity. The results exhibit that the properties of the fabricated configurations can be effectively modulated. The graphene/silicon heterostructures with a Si (111) interface and high resistivity show a better photovoltaic behavior and should be applied for high-performance photodetectors. With the combined atomic force microscopy and theoretical analysis, the possible origination is discussed. The work here should be helpful on exploring high-performance graphene/silicon photoelectronics.

1. Introduction

Graphene, a single-atom-thick sheet of arrayed hexagonal sp^2-bonded carbon atoms, has excellent mechanical flexibility, outstanding optical transparency and high electronic transport properties, making it a promising material for the flexible transparent electrodes [1–8]. The conductivity of graphene has been predicted to be as low as 30 Ω/□ with a visible light transmittance of 97.7%, which is much better than the currently used commercial transparent electrodes of indium doped tin oxide (ITO, typically 30–80 Ω/□ with a visible light transmittance of 90%) [7–9]. Moreover, compared with ITO, graphene has obvious advantages such as abundance of raw materials on earth, acid and alkaline-resistance, and transparency in near infrared region [10]. Therefore, graphene has stimulated intense studies on its potential application for transparent electrodes since its discovery [11–15].

As transparent electrodes, graphene has been applied for variable optoelectronics, including solar cells, light-emitting diodes (LEDs), and photodetectors [10,16–20]. On the other hand, silicon (Si) is widely used for optoelectronic devices in industry owing to its outstanding optoelectronic performance. Graphene/silicon (Gr/Si) configurations for optoelectronics have thus drawn considerable attention. Because of the work function difference between graphene and silicon, their contact results in charge transfer, yielding a built-in electric field [21–24]. While the configuration is illuminated, light could pass through graphene onto silicon. The sunlit silicon absorbs photons and generates electron–hole pairs, which are separated by the built-in electric field. Graphene and silicon collect the separated holes and electrons, respectively. Gr/Si configurations are use of this principle to have been demonstrated as solar cells or photodetectors. It is reported that Gr/Si Schottky junctions as solar cells could convert the energy with efficiency of 1.7% [25]. When graphene was doped with bis-(trifluoromethanesulfonyl) amide, the conversion efficiency of the solar cell could achieve 8.6% [26]. A colloidal antireflection coating and nitric acid doping graphene could enhance the efficiency to 14.5% [27]. In addition to solar cells, Gr/Si configurations applied in photodetection also made great progress [28–30]. It is reported that Gr/Si junctions indicate a potential use as ultrasensitive photodetectors thanks to the excellent weak-signal response with photovoltage responsivity exceeding 10^7 V/W [29]. These intriguing results raise a further study of the properties of Gr/Si configurations to improve their performance for the future applications.

Here, through varying the silicon contacted crystal face or the silicon resistivity, we fabricated different Gr/Si configurations and systematically studied their electrical properties including ideality factor (n), barrier height (Φ_B), and series resistance (R_S) under dark condition and photoelectrical performance of open-circuit voltage (V_{OC}) and short-circuit current (I_{SC}) under light illumination.

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Based on these studies, we further explored their applications for photodetectors.

2. Experimental details

2.1. Graphene synthesis and characterizations

Graphene sheets were synthesized with a chemical vapor deposition (CVD) method by using methane (CH_4) as source material and 25-μm-thick Cu foils (Alfa Aesar, item No. 13382) as substrates in a horizontal quartz tube furnace [31]. Firstly, the furnace was heated up to 1000 °C and evacuated to less than 10 Pa. Cu foils were then moved into the center of the quartz tube furnace and annealed for 30 min under the protection of 100 sccm H_2 gas flow. In the following 7 sccm CH_4 was introduced in the tube for another 30 min to synthesize graphene. In the whole Cu foils annealing and graphene growth progress, the temperature of the furnace remained at 1000 °C. To get free-standing graphene films, the graphene/Cu foils were spin-coated with poly-methyl methacrylate (PMMA) on the upper and baked at 120 °C for 1 min. Graphene films on the other side of the Cu foils were cleaned by O_2 plasma and the Cu foils were etched by 0.1 M $(NH_4)_2S_2O_8$ [32]. When Cu was completely dissolved, as-obtained graphene/PMMA films were rinsed thoroughly with deionized (DI) water for the following use.

2.2. Graphene/silicon heterostructure fabrication

Three kinds of *n*-type silicon wafers covered with a 300-nm-thick thermal oxide (SiO_2) film were studied due to their different terminated crystal surfaces or doping levels (high or low resistivity). They were Si (111) with a resistivity of 5 Ω·cm (denoted by Si (111)-H), and Si (100) with a resistivity of 5 Ω·cm or of 0.005 Ω·cm (denoted by Si (100)-H or Si (100)-L). The schematic diagram of the device fabrication process is shown in Fig. 1. Firstly, the back side of these silicon wafers was etched by buffered oxide etchant (BOE) and then covered with thermally evaporated Au/Ni films for the back electrodes, which were rapidly annealed to form Ohmic contact with silicon [33,34]. In the front side of the wafers, a pane of Au/Ni film was patterned with photolithography and thermally evaporated as the front electrode. A 0.1 cm^2 area of silicon square window in the center of the front electrode pane was then etched using a photolithography and BOE etching method. After the Si windows were etched thoroughly, they were rinsed with DI water and rapidly covered with the as-produced graphene/PMMA films. Then, the samples were laid overnight in the air, and dried in vacuum for 5 h. Finally, PMMA layers were thoroughly dissolved by acetone at 55 °C for 4 h and nitrogen gas was used to dry the samples.

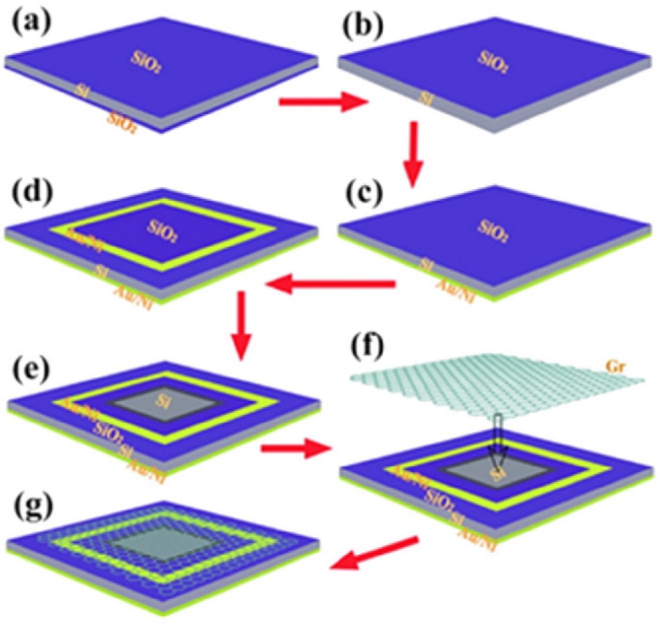

Fig. 1. Schematic diagram of the graphene/silicon Schottky junction fabrication process. (a) The source material of silicon with 300-nm-thick thermal oxide film on both sides. (b) The SiO_2 on the back of Si wafer is totally etched by buffered oxide etchant (BOE). (c) Au/Ni film is thermally deposited on the etched Si, and then annealed rapidly to form Ohmic contact to the Si. (d) Au/Ni frame electrode is thermally deposited on the SiO_2 on the front of the wafer by using photolithograph and lift-off method. (e) An area of 0.1 cm^2 SiO_2 is totally etched by BOE in the center of the electrode frame. (f) Graphene is transferred on the Si wafer. The graphene totally covers the exposed Si and contacts the electrode frame. (g) The final graphene/Si configuration obtained.

2.3. Characterization

The electrical and photoelectrical properties of Gr/Si configurations were characterized with a Keithley 4200-SCS semiconductor analyzer at room-temperature in atmosphere. The light source was an adjustable light-emitting diode (LED) lamp whose power can be tuned. We used an optical power meter of SGN-1 to calibrate the power of the LED and calculated the incident power on the configurations based on their effective area. The Raman spectra were characterized on a Horiba Jobin Yvon LabRAM HR800 Raman system with 514-nm laser excitation. The surfaces of silicon were imaged using atomic force microscopy (AFM—Bruker Dimension Edge SPM System). All measurements were performed at room temperature and in ambient air.

3. Results and discussion

Fig. 2a demonstrates a typical photograph and schematic plans of the produced Gr/Si configurations. Graphene film can be clearly seen from the photograph. Fig. 2b shows typical Raman spectra of the graphene on the etched silicon windows in three different kinds of Gr/Si heterostructures. The 2D band is symmetric and much higher than the G band in all of the samples, indicating that the graphene is monolayer graphene [31]. The intensities at around 1430 cm^{-1} are from the underneath Si, which demonstrate that the graphene is indeed on the etched Si [35].

Fig. 3a shows typical *I*–*V* curves of the three different kinds of Gr/Si heterostructures under dark condition. It can be seen from Fig. 3a that the underneath Si and the graphene form typical Schottky contact in all of the Gr/Si heterostructures. However, their rectifying behaviors exhibit different features. Gr/Si (111)-H structure depicts a higher reverse leakage current, and Gr/Si (100)-L junction shows the highest forward current. These differences are perhaps due to their different intrinsic parameters, including ideality factors (n), barrier heights (Φ_B) and series resistances (R_S), which could be extracted from the characteristic *I*–*V* curves using the following method.

The forward current through a Schottky junction follows the thermionic emission model, which can be represented by [36]:

$$I = I_S\left[\exp\left(\frac{eV_D}{nkT}\right)-1\right] \quad , \qquad (1)$$

$$V_D = V - IR_S, \qquad (2)$$

where I_S is the reverse saturation current, e is the electronic charge, V_D is the bias voltage across the Schottky junction, n is the ideality factor, k is the Boltzmann constant, T is the absolute temperature, and R_S is the series resistance. I_S can also be represented by:

$$I_S = A_{eff}A^{**}T^2\exp\left(-\frac{e\Phi_B}{kT}\right) \quad , \qquad (3)$$

where A_{eff} is the effective area of Schottky junction, A^{**} is the Richardson constant, and Φ_B is the Schottky barrier height. Using current density J