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Diffusion barrier property of $MnSi_xO_y$ layer formed by chemical vapor deposition for Cu advanced interconnect application

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ABSTRACT

An amorphous manganese oxide layers formed by chemical vapor deposition have been studied as a copper diffusion barrier. The thermal stability of the barrier layer was assessed by annealing $Cu/MnSi_xO_y/SiO_2/Si$ samples at 400 °C for various times up to 10 h. Transmission electron microscopy, energy-dispersive X-ray spectroscopy (EDX), secondary ion mass spectroscopy (SIMS), capacitance-voltage and current–voltage measurements were performed. Failure of the barrier property is marked by observing the copper peak appearing in EDX and SIMS spectra data from the SiO_2 region. Amorphous $MnSi_xO_y$ barrier with a thickness of 1.2 nm has failed in preventing Cu diffusion into SiO_2 substrate after anneal at 400°C in vacuum for 1h, as proven by the presence of Cu in the dielectric (SiO_2) layer. However, the amorphous $MnSi_xO_y$ with the thickness of 2.0 nm barrier was thermally stable and could prevent Cu from inter-diffusion to the SiO_2 substrate after annealing at 400 °C even up to 10 h.

1. Introduction

As feature sizes in ultra-large scale integration microelectronic devices continue to shrink, the resistance–capacitance delay becomes a limiting factor in the speed performance of these devices. The transition from Al- to Cu-based interconnects is essentially motivated by the fact that Cu has lower resistivity and superior electromigration resistance vs. Al. However, since Cu diffuses rapidly into Si and SiO_2, and it forms Cu silicides at temperatures as low as 200 °C, the requirement of an effective barrier layer is vital. The barrier layer should have high thermal stability and low resistivity, and show a strong adhesion with Cu and Si [1]. In addition, to maintain the effective resistivity at a low constant value of 2.2 μΩ cm, the barrier thickness should be as thin as possible. According to the node scaling rule, a decrease in barrier thickness from 2.6 to 1.9, to 1.2 nm is required for the 32, 22 and 13 nm technology nodes, respectively [2]. Bilayers of Ta/TaN have been widely used as diffusion barriers for Cu metallization [3]. However, the conventional barrier formation methods have begun to face technological limitations in the advanced technology node because the barrier layer thickness on the side wall of trenches and vias is too thin to ensure the barrier property.

A self-formed barrier layer of Mn oxide formed by physical vapor deposition (PVD) of Cu–Mn on tetraethylorthosilicate (TEOS)–SiO_2 has been proposed by Koike et al. [4,5]. Formation of a thin Mn oxide layer in the range of 2 to 8 nm could be obtained by modifying the annealing condition of the as-deposited Cu–Mn film. A 7 nm-thick Mn oxide layer was shown to remain stable for 100 h at 450 °C annealing and for 10 h at 600 °C in vacuum. In addition, a 2.5 nm-thick Mn oxide layer indicates a good barrier property without inter-diffusion of Cu into the SiO_2 layer after annealing in vacuum at 450 °C for 5 h [4]. Since PVD method has poor step coverage in decreasing trench size, there is a need to develop an equivalent process using chemical vapor deposition (CVD) so that formation of an overhung region in small feature size and high aspect ratio structures is avoided [6].

Wen-bin et al. reported metallic manganese layer formation by thermal CVD above 410 °C using methylcyclopentadienyl tricarbonyl manganese, $(MeCp)Mn(CO)_3$, as a precursor [7]. They found that 50% of the precursor was decomposed at 440 °C. Neishi [8] also reported metallic manganese formation in an aggregated island form using CVD at 500 °C and bis(ethylcyclopentadienyl) manganese. Below 400 °C, a thin and uniform Mn oxide layer was formed when the process was carried out on TEOS–SiO_2 [8,9]. The Mn oxide layer was found to show a good adhesion with the Cu over-layer. It also showed a good step coverage and low carbon content when it was deposited below 300 °C [9,10]. Good barrier properties against Cu diffusion were also reported for layer thicknesses of 4.2 and 2.6 nm by annealing at 400 °C for 100 h and under bias temperature annealing at 3 MV/cm and 277 °C for 6×10^3 s [8,10]. In addition, the Mn oxide layer was shown to be an excellent barrier property against H_2O and O_2 diffusion from a dielectric substrate, thus preventing the oxidation of a Cu overlayer [11,12].

It was found that the structure and thickness of the Mn oxide layer formed by CVD on SiO_2 were dependent on the amount and types of the adsorbed moisture in the SiO_2 substrate [8,13]. A Mn oxide layer formed on an as-received substrate was composed of a bilayer of crystalline MnO_x on the top surface and amorphous $MnSi_xO_y$ at the bottom adjacent to the substrate. On a pre-annealed substrate, only the amorphous $MnSi_xO_y$ layer was formed and its thickness was decreased

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from 8.0 to 1.8 nm by increasing pre-annealing temperature from 150 to 500 °C. These results would allow us to investigate the diffusion barrier property of $MnSi_xO_y$ with various thicknesses and structures on the TEOS–SiO_2 substrate. So far, a good diffusion barrier property was shown for the $MnSi_xO_y$ having the thicknesses of 2.6 nm and 4.2 nm. However, the minimum possible thickness is not known for the $MnSi_xO_y$ layer to act as a diffusion barrier layer. In this paper, we explore the minimum possible thickness for $MnSi_xO_y$ to act as an efficient diffusion barrier layer.

2. Experimental details

The substrates used in this study were 50 nm-thick TEOS-SiO_2 on p-type doped Si wafers. First, they were pre-annealed at 300 or 400 °C under pressure of 1.0×10^{-5} Pa for 30 min using an infrared furnace. The heating rate applied for the pre-annealing temperatures was 0.78 °C/s. Subsequently, a thin Mn oxide layer was deposited on the pre-annealed substrates by CVD at 300 °C for 30 min using H_2 as a carrier gas and bis(ethylcyclopentadienyl) manganese – $(EtCp)_2Mn$ – as a precursor. The details of this particular CVD process were described elsewhere [8]. On the Mn oxide layer, a 100 nm-thick Cu layer was then deposited in situ in a physical vapor deposition (PVD) chamber, which is connected to the same cluster as the CVD deposition cell. In this way, air exposure for the Mn films was avoided. Besides blanket samples, metal-oxide-semiconductor (MOS) capacitor structures were also made following the same sequences and processes. The $200 \times 200\ \mu m^2$ top Cu electrode of the MOS capacitor was formed by a photolithographic process using HNO_3 solution as a wet-etchant forming a pad. For the bottom electrode of the MOS capacitor, a blanket layer of 100 nm-thick Al was deposited on the other side of Si (100) wafer. Then, the samples were annealed at 350 °C for 1 h in vacuum to make Ohmic contact between Si and Al. These samples were designated as reference samples. For both the MOS capacitor and the blanket samples, the diffusion barrier property of the Mn oxide layer was assessed by a post-annealed at 400 °C in high vacuum for various time lengths of 1, 4 and 10 h.

Microstructure and composition analyses were performed on the blanket samples before and after the post-annealing by transmission electron microscopy (TEM) at 200 kV and X-ray energy dispersive spectroscopy (EDX) using a Hitachi HF-2000EDX. The depth concentration profiles of each element Cu, Mn, Si and O for both the reference and post-annealed samples were obtained by secondary ion mass spectroscopy (SIMS) on a CAMECA IMS-7f with Cs primary ions accelerated at 5 kV. Note that SIMS spectra were obtained by ion sputtering the sample from the Si side to reduce the artificial penetration of the constitutive elements in the direction of the ion beam. Therefore, it is possible to evaluate the diffusion barrier property of the barrier layer by the presence or absence of the metallic elements in the SiO_2 layer. The capacitance–voltage (C–V) and current–voltage (I–V) characteristics were measured on the MOS capacitors using a microprobe system connected to an Agilent 4155C parametric analyzer and a Solartron 1260 impedance/gain-phase analyzer.

3. Results and discussion

Fig. 1(a)–(c) shows cross-sectional TEM images of the reference sample and the post-annealed samples at 400 °C for 10 and 60 min, respectively. Substrate pre-annealing was performed at 400 °C for 30 min. All the TEM images show a uniform interface layer between Cu and SiO_2. From our previous study [13,14], this layer has been confirmed to be an amorphous $MnSi_xO_y$ layer. While the thickness of the $MnSi_xO_y$ layer is 1.2 nm in the reference sample, the thicknesses measured for the films after annealing at 10 and 30 min were 1.1 and 1.5 nm, respectively. Considering a TEM measurement error of ±0.2 nm, the thickness of the Mn oxide layer appears to be unaffected by annealing under the conditions described above. The EDX spectra taken from the SiO_2 layer of each sample are shown in Fig. 1(d). No manganese peak is observed in all spectra. However, a copper peak can be observed in the post-annealed sample for 60 min, indicating the inter-diffusion of Cu through the $MnSi_xO_y$ to the SiO_2 substrate. Therefore, this result suggests that the 1.2 nm-thick Mn oxide layer is too thin to be consider as an efficient diffusion barrier for Cu interconnect applications.

Next, the diffusion barrier property of a thicker $MnSi_xO_y$ layer, i.e. 2 nm, is investigated. In this case, the substrates were pre-annealed at 300 °C for 30 min. Fig. 2(a)–(c) shows cross-sectional TEM images of the reference sample and the post-annealed samples at 400 °C for

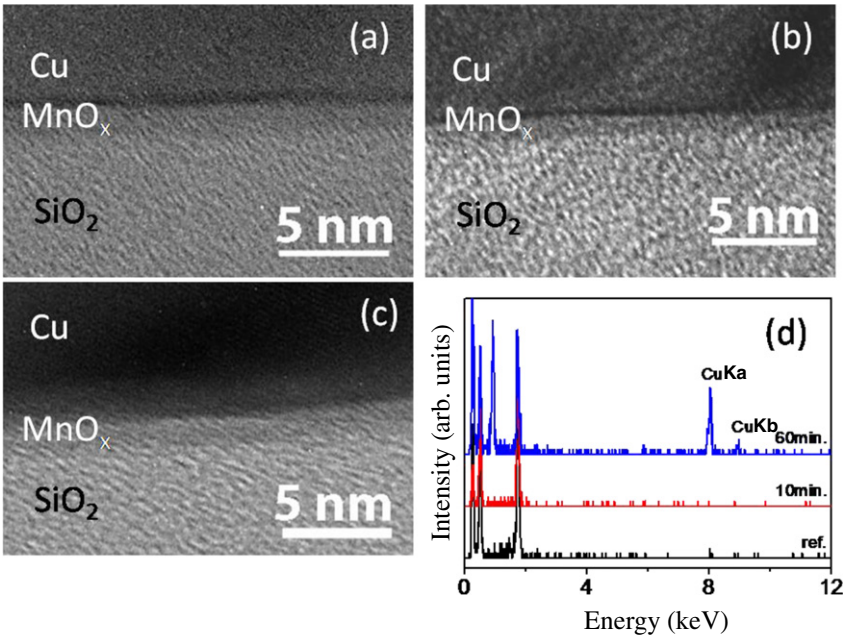

Fig. 1. (a–c) TEM images of Cu/MnO_x/SiO_2; (a) a reference sample having a 1.2 nm thick MnO_x layer, (b) an annealed sample at 400 °C for 10 min, and (c) an annealed sample at 400 °C for 60 min. (d) EDX spectra of each sample taken from the SiO_2 substrate.