



Comparison of high- κ Nd_2O_3 and NdTiO_3 dielectrics deposited on polycrystalline silicon substrates

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ABSTRACT

High- κ Nd_2O_3 and NdTiO_3 films deposited on polycrystalline silicon treated at various post-rapid thermal annealing temperatures were fabricated as high- κ gate dielectrics. The NdTiO_3 samples demonstrated a higher effective dielectric constant, lower leakage current, higher breakdown electric field, smaller gate voltage shift, and lower electron trapping rate than the high- κ Nd_2O_3 polyoxide dielectric samples. Annealing effects were analyzed using electrical measurements and multiple material analysis techniques included X-ray diffraction and atomic force microscopy. Incorporating Ti content into Nd_2O_3 dielectrics resulted in noticeable improvements in electrical performance and material quality. Results indicate that NdTiO_3 dielectrics show promise for future high- κ dielectric electronic device applications.

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1. Introduction

As the size of traditional SiO_2 gate oxide has shrunk, reliability issues have become a concern due to the increased potential of dielectric breakdown caused from ultrathin gate dielectric layers [1,2]. In recent years, lanthanide oxides such as Er_2O_3 [3], Sm_2O_3 [4], and Gd_2O_3 [5] have emerged to replace SiO_2 as the gate oxide for their high dielectric constant compared to silicon oxide (high- κ) and large band offset with silicon. The main advantage of a high- κ dielectric is an equivalent capacitance value in a physically thicker film so that the possible dielectric breakdown and large leakage current can be avoided [6]. However, reliability problems arise, such as interfacial defects that include dangling bonds and traps between the high- κ oxide and the substrate. Therefore, it is worthwhile to investigate high performance dielectrics comprised of various material compositions, alternative processes, and treatments. As for complementary metal–oxide–semiconductor applications, the single Si crystalline substrate is more preferable [7] but for the thin film transistor (TFT) applications, the polysilicon substrate is more applicable [8] because the polyoxide substrate exhibits low conductivity, high breakdown, and high-charge-to-breakdown properties [9]. In this study, the interdielectric polyoxide with potential TFT applications has been used to replace the traditional single-crystal Si substrate.

In this study, Nd_2O_3 was combined with Ti atoms to form a NdTiO_3 high- κ dielectric layer on a polyoxide substrate [10]. Titanium oxide was chosen because it has a very high- κ value of 80, and incorporating Ti atoms could potentially increase the dielectric strength and suppress low- κ oxide formation [11]. As the film was further treated with post rapid thermal annealing (RTA), unwanted suboxides could be eliminated, thereby improving dielectric quality. After the material quality is improved, leakage current decreases, while breakdown electric field and voltage both increase. In our fabrication, we sputtered a high- κ NdTiO_3 dielectric on top of a polyoxide substrate. To examine improvements caused by the addition of Ti atoms and annealing, material analyses including X-ray diffraction (XRD) and atomic force microscopy (AFM) were performed. Electrical characterizations were conducted to examine the dielectric performance.

2. Experimental

Nd_2O_3 and NdTiO_3 polyoxide capacitors were fabricated on n^+ -polysilicon/oxide/p-type silicon substrates. With the addition of Ti into Nd_2O_3 , the high- κ Nd_2O_3 and NdTiO_3 polyoxide capacitors were compared. At first, the p-type silicon wafer was cleaned with a regular RCA cleaning process and dipped in a diluted hydrofluoric acid solution to remove the native oxide. An oxide layer of 600 nm in thickness was grown by thermal oxidation on the p-type silicon. Then, a polysilicon film of 300 nm in thickness was deposited at 625 °C by a low pressure chemical vapor deposition system. The polysilicon/oxide/p-type silicon

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substrates were annealed at 950 °C to activate the substrate and reduce resistance. For the Nd_2O_3 capacitor, a Nd_2O_3 film 27 nm in thickness was deposited by RF sputtering in diluted O_2 ($\text{Ar}/\text{O}_2 = 12.5/12.5$) with an ambient sputtering power of 150 W and an operating pressure of $\sim 1.5 \times 10^{-4}$ Pa. The distance between the target and the substrate was around 10 cm and the sputtering rate was around 2.6 nm/min. Then, post-annealing was performed in N_2 ambient at different annealing temperatures for 30 s by RTA at 600 °C, 700 °C, 800 °C, and 900 °C [12]. As for the NdTiO_3 film, a Nd_2O_3 film of 18 nm in thickness was deposited by RF sputtering in diluted O_2 ($\text{Ar}/\text{O}_2 = 12.5/12.5$) with an ambient sputtering power of 150 W, with an operating pressure at $\sim 1.5 \times 10^{-4}$ Pa. A Ti film 9 nm in thickness was deposited by RF sputtering with an ambient sputtering power of 150 W and an operating pressure at $\sim 1.5 \times 10^{-4}$ Pa. Post-RTA was done in O_2 ambient for 30 s, with RTA at temperatures of 600 °C, 700 °C, 800 °C, and 900 °C. After annealing, a NdTiO_3 film was formed. After the Nd_2O_3 and NdTiO_3 films were annealed, a 3000 Å Al gate electrode was deposited using a thermal evaporator. The capacitor area was defined by wet etching and HF:deionized water (1:10) was used to etch away Nd_2O_3 and NdTiO_3 in the fabrication process. The Nd_2O_3 and NdTiO_3 polyoxide capacitor cross-sections are shown in Fig. 1(a) and (b), respectively. Prior to depositing the blocking oxide layer, the high- κ dielectric layer was examined using XRD and AFM to analyze the material properties. The make and model of XRD were Bede X-ray Metrology and Bede D1. The X-ray source was $\text{Cu K}\alpha$ ($\lambda = 1.542$ Å) and the configuration was Bragg–Brentano theta-2 theta. The system used a grazing incidence angle ($\theta = 0.5^\circ$) in the diffraction and the diffraction angle 2θ range was from 20 to 60°. The surface morphologies were measured by a Veeco D5000 AFM in

tapping mode using an applied nano-silicon tip with a 50 N/m spring constant. The scan rate used was 1 Hz and the scan area was $2 \mu\text{m} \times 2 \mu\text{m}$ with a set engagement ratio of 80%. After the dielectric was fabricated, the equivalent oxide thicknesses (EOTs) of the high- κ Nd_2O_3 and NdTiO_3 dielectric were determined by high-frequency (100 kHz) capacitance–voltage (C–V) measurement by using HP-4284, Hewlett-Packard, USA. The current density versus electric field (J–E) characteristics were measured using a HP4200 semiconductor parameter analyzer.

3. Results and discussion

To examine material improvements caused by annealing, XRD analysis was used to monitor the crystalline structure. The crystalline Nd_2O_3 phase was observed for samples annealed at different temperatures, and characteristic XRD peaks can be seen in Fig. 2(a). Three diffraction peaks (002), (102) and (110) are clearly presented at 29.7°, 40.4° and 47.8°. Therefore, at the post-RTA temperature of 900 °C, the peak intensity is strongest. In addition, the sample with the highest RTA temperature (900 °C) clearly exhibits an extremely strong peak characteristic of (102)-oriented Nd_2O_3 , demonstrating well-crystallized and strong Nd_2O_3 structures for high- κ Nd_2O_3 dielectrics with post-RTA treatment. To examine the XRD of NdTiO_3 film after post-RTA annealing at various temperatures in O_2 ambient for 30 s, Fig. 2(b) shows XRD patterns of the addition of a titanium metal layer to neodymium oxide films before and after the post-deposition annealing treatment. Diffraction peaks of NdTiO_3 at (220) and (023) are clearly presented at 46.2° and 48°. The peak intensity of the NdTiO_3 compound became stronger as the annealing temperature was increased to 800 °C, but suddenly decreased at 900 °C. This finding suggests that the Ti atoms could not obtain enough of a kinetic energy reaction with Nd_2O_3 to form a better NdTiO_3

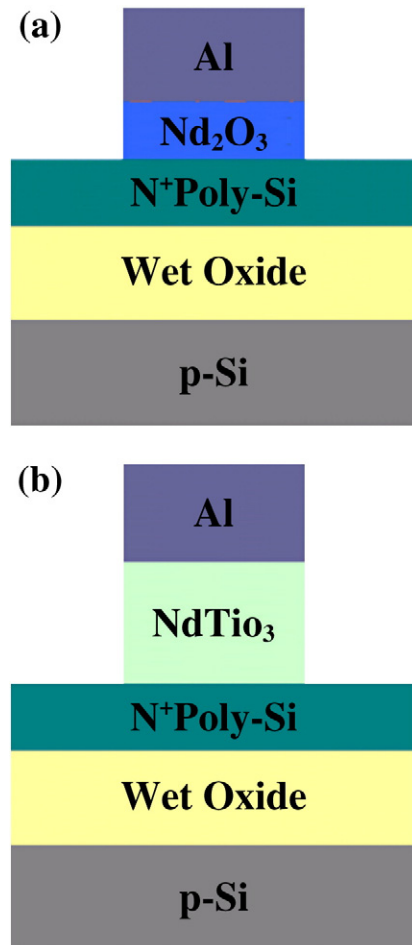


Fig. 1. (a) Nd_2O_3 polyoxide capacitor structure. (b) NdTiO_3 polyoxide capacitor structure.

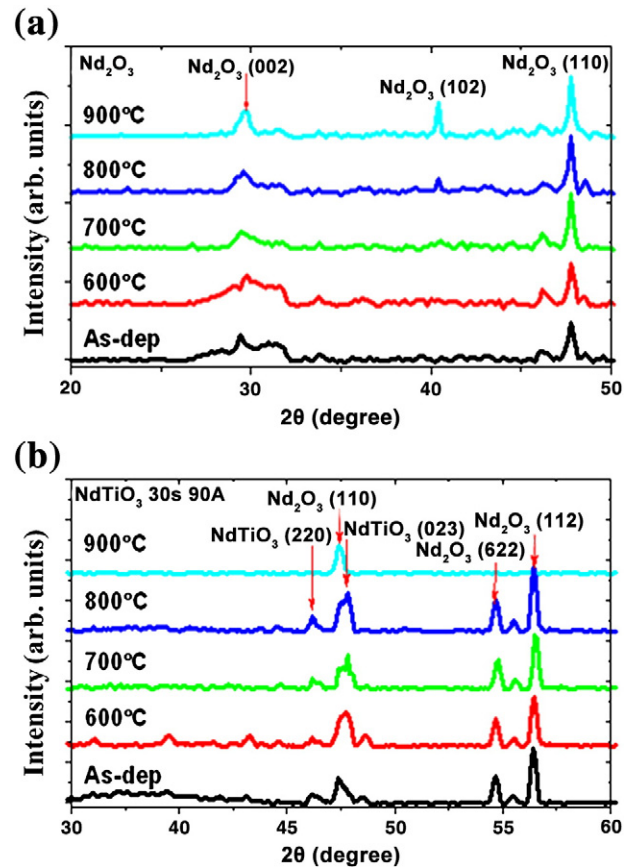


Fig. 2. (a) XRD patterns of the Nd_2O_3 film after annealing at various temperatures. (b) XRD patterns of the NdTiO_3 film after annealing at various temperatures.

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