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# Temperature dependence of the electrical characteristics of low-temperature processed zinc oxide thin film transistors

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ABSTRACT

The impact on the electrical behavior of thin film transistors, TFTs, based on zinc oxide, ZnO-based TFTs, with temperature is analyzed. ZnO is deposited using pulsed laser deposition techniques and the temperature used during the entire fabrication process is kept below 100 °C. Up to 330 K, the transfer curves practically remain constant or slightly shifted toward more positive voltages. For temperatures up to 330 K, they show the combined effect of the threshold voltage shifting toward more negative voltages and the increase of series resistance. The drain current shows an Arrhenius-type dependence with temperature in subthreshold regime with activation energy of around 0.53 eV. In above threshold regime, for temperatures above 330 K, the activation energy is around 0.15 eV.



## 1. Introduction

Oxide semiconductor thin film transistors, OSTFTs, have made an impressive progress particularly in display applications in a relatively short time [1]. Among the advantages of these devices are their high optical transparency [2,3], a relatively high electron mobility [4], as well as the possibility of using low temperature and relatively low cost processing techniques [1,3].

Although initial attempts of using zinc oxide, ZnO, as active layer appeared during the 60s [5], the birth of transparent electronics is normally associated with ZnO TFTs presented in 2003, when transparent conductive oxide based electrodes and mobility as high as 2.5 $cm^2 V^{-1} s^{-1}$, were reported [2]. However, some of these approaches utilize high post-processing temperatures incompatible with emerging low-temperature flexible electronics [6,7]. Not to mention, some of them use very crude patterning techniques (e. g. shadow mask or common back gate contact), which prohibit the implementation and optimization of high performance circuits [2,8]. An important step in advance was the development of fabrication techniques, using low or even room temperature processes [1,3,8].

Regarding the electrical characteristics of OSTFTs, much interest has been dedicated to increase mobility, as well as the stability of the devices. To increase stability, amorphous multi-component oxide layers containing indium–gallium–zinc oxides, IGZO, or hafnium–indium–zinc oxides, HIZO, have been studied [1,9]. The temperature, *T*, behavior of the electrical characteristics, however, has not been sufficiently studied. Some articles presenting the behavior of OSTFTs with temperature can be found, but usually, they cover temperatures below 300 K [10–12].

In this work we analyze the behavior in the temperature range of 300 K to 370 K, of the electrical characteristics of ZnO TFTs fabricated with temperature processes not exciding 100 °C. Possible causes for the observed effects are discussed.

## 2. Experimental part

ZnO TFTs with the bottom-gate top-contact configuration shown in Fig. 1a were fabricated as reported in [3]. The process consists of 100 nm of patterned gold film to serve as a gate metal. The hafnium oxide, $HfO_2$, dielectric layer is deposited by atomic layer deposition at 100 °C and patterned with a buffered oxide etch solution. The ZnO layer is deposited by pulsed laser deposition and subsequently covered by 500-nm of poly-p-xylylene-C (Parylene-C) deposited by chemical vapor deposition at room temperature, which is used as a protective/hard-mask film. Source and drain vias are opened through the hard-mask film using reactive ion etch. The next step is to deposit 100 nm of aluminum layer that will serve, after a photolithographic process, as the source and drain contacts. Fig. 1b shows an optical micrograph of

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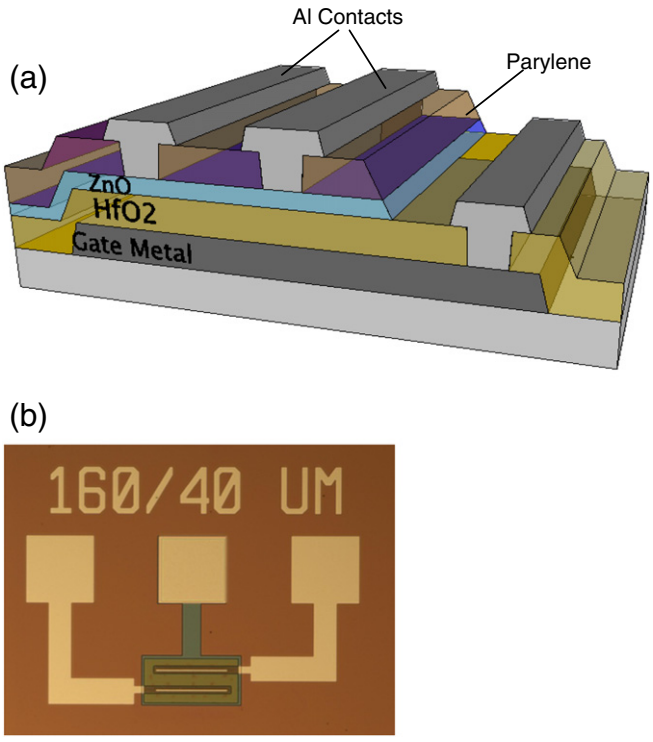


**Fig. 1.** a) Cross section of the analyzed ZnO TFT; b) optical micrograph of a TFT.

an actual TFT. TFTs with different channel widths ($W = 40$, 80 and 160 μm) and channel lengths ($L = 20$, 40 and 80 μm) are included in each die.

Electrical measurements at different temperatures were done in dark and in vacuum conditions, using a K20 programmable temperature controller and measurement chamber from MMR Technologies Inc. and a Keithley 4200 semiconductor characterization system.

The linear transfer curves and transfer curves in saturation, as well as the output characteristics for devices with different $W/L$ ratios were measured in the temperature range between 300 K and 370 K, making sure that the variation of the drain current, $I_{DS}$, was due to the temperature variation and not to instability effects. Since the characteristics for all devices showed a similar behavior, results will be analyzed for a device with $W = 160$ μm and $L = 40$ μm.

## 3. Analysis and discussion of results

Analyzing the electrical characteristics of the fabricated TFTs, it was observed that during the first measurements at room temperature, the devices presented threshold voltage, $V_T$, instability. For this reason, measurements with temperature were done after several consecutive measurements, until the devices were stabilized and measurements at room temperature repeated.

Fig. 2a and b shows the linear transfer characteristics measured in the temperature range between 300 and 370 K. It is seen that, as the temperature is increased up to around 330 K, the transfer curves practically remain constant or shift slightly toward more positive voltages, see Fig. 2a. As the temperature is further increased, the curves shift toward negative voltages. At the same time, up to $T = 340$ K and for gate voltages, $V_{GS}$, greater than 5 V, an increase of the channel and series resistance, $R_S$, is observed, represented by the decrease of the drain current, $I_{DS}$, as the temperature is increased. For higher temperatures, the maximum value of $I_{DS}$ tends to saturate and the gate voltage at which this saturation appears is reduced.

In Fig. 2b, the same curves are plotted in a semilog scale to see in more detail the $V_T$ shift with temperature. In Fig. 3, a similar behavior of $V_T$ is observed for the transfer curve in saturation, although the shift to the left is smaller.

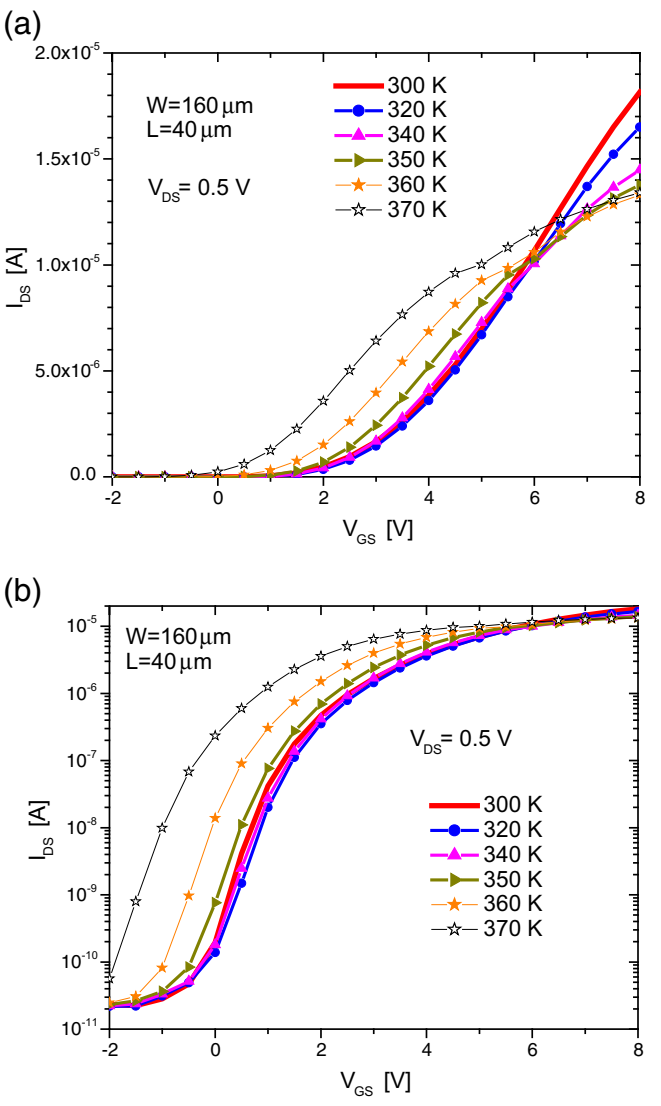


**Fig. 2.** Linear transfer characteristic at $V_{DS} = 0.5$ V in the temperature range from 300 K to 370 K: a) natural plot; b) semilog plot.

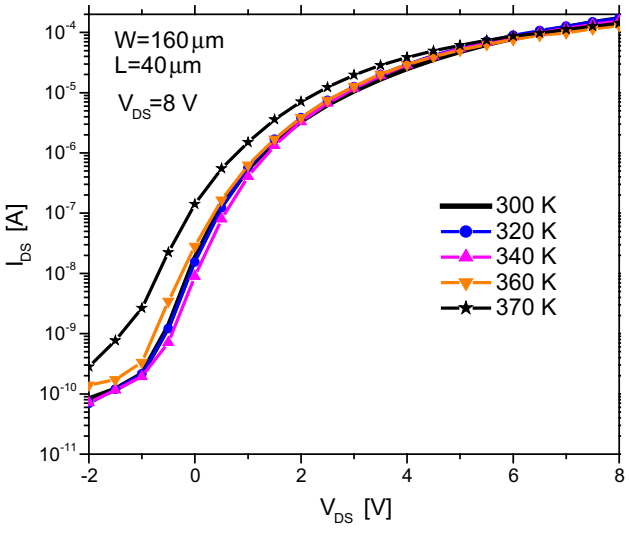


**Fig. 3.** Saturation transfer characteristic at $V_{DS} = 8$ V in the temperature range from 300 K to 370 K in semilog plot.