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Roll-to-roll compatible organic thin film transistor manufacturing technique by printing, lamination, and laser ablation

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ABSTRACT

We present roll-to-roll printing compatible techniques for manufacturing organic thin film transistors using two separately processed foils that are laminated together. The introduction of heat-assisted lamination opens up possibilities for material and processing combinations. The lamination of two separately processed substrates together will allow usage of pre-patterned electrodes on both substrates and materials with non-compatible solvents. Also, the surface microstructure is formed differently when laminating dry films together compared to film formation from liquid phase. Demonstrator transistors, inverters and ring oscillators were produced using lamination techniques. Finally, a roll-to-roll compatible lamination concept is proposed where also the *source* and *drain* electrodes are patterned by laser ablation. The demonstrator transistors have shown very good lifetime in air, which is contributed partly to the good material combination and partly to the enhanced interface formation in heat-assisted lamination process.

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1. Introduction

In a roll-to-roll printing process, organic electronic devices are made typically with additive processes, i.e., the layers are printed on top of each other. Printing techniques are similar for all polymer devices (e.g. transistors, light emitting diodes [1], solar cells [2], sensors [3] and they all have the same principle limitations, although the most critical limiting restriction may be different. The transistor is a basic electronic component that can be used to very sensitively probe the different limitations of the manufacturing process, such as thin film layer thickness, morphology and roughness, feature size and registering accuracy. The basic device concept is described by Sze [4] and reviewed from a conjugated polymer and oligomer perspective by Horowitz [5–7]. Polymer transistor processing follows the same design rules as other printed devices. All layers of an organic thin film transistor (OTFT) can be printed [8], adding one patterned layer on top of another. However, the limited resolution of the printing processes limits the performance of such devices. In order to achieve better performance, the electrode dimensions and layer thicknesses must be small, and the *gate* to *source*/*drain* electrode overlap must be minimized. One approach is to use a pre-processed and pre-patterned [9] substrate with metal (or e.g. conductive transparent *indium tin oxide* (ITO) electrodes. A plastic substrate can have etched metal features with high definition providing excellent base onto which to build the device. After deposition of the active printed layers, the top electrode must be deposited. In *top gate* configuration, the need for resolution is not so strict; therefore, the *gate* electrode can be printed. However, the capacitance resulting from the gate-source/drain electrode overlap is a major component in limiting the switching speed of the transistor. Furthermore, some of the active layers may not be compatible with the following printing step, or a high-definition and high-conductance top electrode is needed. For this case, we introduce a lamination technique.

The lamination of a protective barrier foil is typically used as the last finishing step of the device fabrication [10,11]. It has been shown to enhance lifetime of organic transistors [12]. However, the active layers can be laminated [13]. Lamination has been used in a *pentacene* OTFT when the interface was studied with *quartz* or *silicon* substrates [14] or with polydimethylsiloxane stamps [15,16]. Another author uses lamination to make the electrode contacts for transistors [17,18]. Semiconducting single crystals [19] or sheets [20] have been laminated on silicon wafers. Here we present the lamination of two plastic sheets with pre-patterned electrodes, with one containing the polymer semiconductor and another containing the polymer dielectric. By introducing heat and pressure, the sheets make the contact between the polymer layers. This technique allows the usage of materials with non-compatible solvents (no need for orthogonal solvent) [20]. It allows the use of pre-patterned (metal) electrodes on both sides. The active layers are automatically shielded by the two substrates. Also the surface microstructure is formed differently when laminating dry films together compared to film formation from solvent [14]. Lamination-induced mobility increase in OTFTs, attributed to surface smoothening and

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relaxation of crystalline *pentacene* films, has been reported by Tunnell et al. [14]. The molecular orientation and packing has improved the mobility when the film is annealed [21] or deposited by solution-shearing [22–24]. In the work by Oh [22], the pressure-assisted thermal cleavage was done as post-treatment for the film, resulting in smoother surface roughness, void space removal, better crystallinity and thus increased mobility. All these reports indicate that the molecular packing can be enhanced in some cases by introducing shearing forces, pressure and/or temperature. This enhancement is studied in our work by comparing laminated devices with ones made with normal deposition methods. Scheme of the lamination process together with materials and printing methods are presented in Figs. 1 and 2. Possible applications could be, e.g., electronic labels and signs with a display element and backplane lamination step (could simplify the process), smart cards and some sensor applications with sensitive layers.

2. Experimental

2.1. Materials

Silicon (Si) substrates with thermally grown silicon oxide (SiO_2) (thickness 300 nm), and patterned gold electrodes were used as rigid substrates. Poly(ethylene terephtalate) (PET) Melinex ST504 DuPont Teijin Films plastic sheets with or without ITO layer were used as flexible substrates. Patterned gold electrodes were either thermally evaporated through a shadow mask or patterned lithographically on the substrates. ITO layer coated on PET substrate was used only for gate electrodes and was not patterned.

Dielectric materials used in the lamination tests were poly(methyl methacrylate) (PMMA) (120,000 Mw), poly(methyl silsesquioxane) (PMSSQ), poly(4-vinylphenol) (PVPh) (25,000 Mw) and poly (melamine-co-formaldehyde) (PMF), a cross-linker for PVPh. Dielectrics and solvents n-butanol, toluene and ethyl diglycol acetate (EDGA) were purchased from Sigma Aldrich.

An undisclosed manufacturer provided a modern amorphous polymer semiconductor. Different versions were used in the initial and the final tests (as an advanced version became available), but for consistency, all the results were compared with reference devices made with the same material version. The comparison of the effects of different processing was thus possible.

2.2. Lamination

Lamination tests were performed with a range of different substrates, materials and configurations (see the materials section) in order to find combinations that result in working devices and a robust laminated structure. In a lamination process, two substrates with varying processed layers were attached together on a hot plate by applying pressure (10–40 kN/m^2) and heat (140-160 °C) for 15–20 minutes. Reference samples without the lamination step were made by spin coating organic layers on Si/SiO_2 substrate, or by printing the dielectric and semiconductor on ITO-coated PET substrate and evaporating top source and drain electrodes. All tests were done manually with small sheets. The roll-to-roll process was not tested due to lack of compatible machinery with high registration requirement.

First lamination tests were done utilizing *n*-type Si substrate with lithographically patterned gold source and drain electrodes, which were laminated on PET substrates featuring an un-patterned ITO conductor as a gate electrode, and gravure printed insulator and semiconductor layers (Fig. 1). Electrical properties of the laminated double gate structure were characterized with gate connected either to the bottom ITO electrode or to the top electrode (conductive n-doped silicon wafer) (Fig. 1). Results were compared respectively to reference devices, which did not utilize the lamination step.

The next step was to replace the rigid silicon wafer with a flexible PET substrate with lithographically patterned *source* and *drain* electrodes (Fig. 2a). Final version of the laminated structure was made by exchanging the ITO coating with a patterned gold electrode which exhibited the additional advantage of being less fragile in the lamination process (Fig. 2b).

After studying the lamination techniques with single transistors, demonstrator inverters and ring oscillators were constructed using two flexible PET substrates. On the first substrate, the gate electrode, dielectric layers and the semiconducting layer were deposited. The second substrate with source-drain electrodes was laminated on top of the semiconductor. The threshold voltage of the transistor was different for PVP:PMF cross-linked dielectric and PMMA/PMSSQ

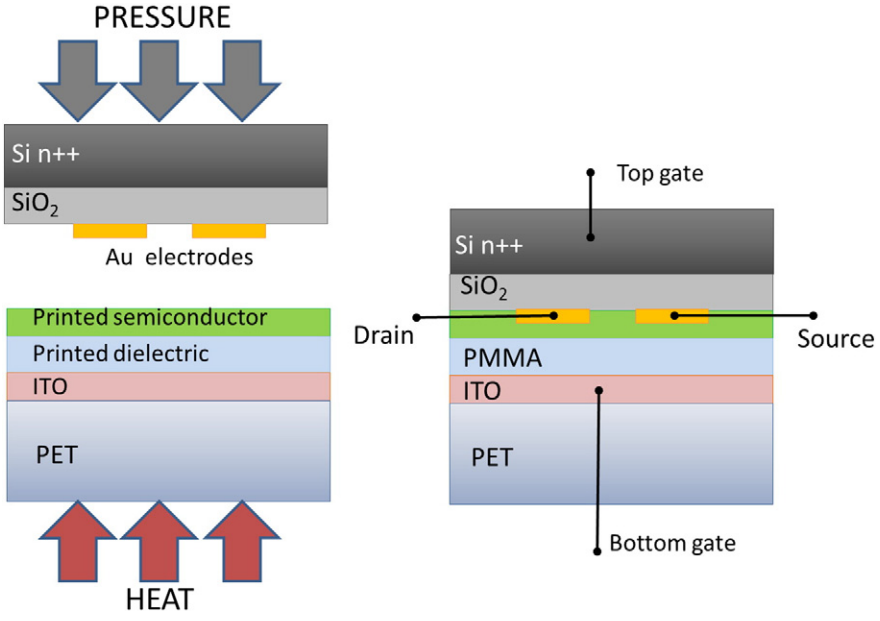

Fig. 1. Schematic picture of the double gate transistor layers and lamination process (left), and double gate transistor electrode configuration (right).

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