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Electrical characteristics of $GdTiO_3$ gate dielectric for amorphous InGaZnO thin-film transistors

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ABSTRACT

In this article, we studied the structural properties and electrical characteristics of $GdTiO_3$ gate dielectric for amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistor (TFT) applications. The a-IGZO TFT device featuring the $GdTiO_3$ gate dielectric exhibited better electrical characteristics, including a small threshold voltage of 0.14 V, a large field-effect mobility of 32.3 cm^2/V-s, a high I_{on}/I_{off} current ratio of 4.2×10^8, and a low subthreshold swing of 213 mV/decade. Furthermore, the electrical instability of $GdTiO_3$ a-IGZO TFTs was investigated under both positive gate-bias stress (PGBS) and negative gate-bias stress (NGBS) conditions. The electron charge trapping in the gate dielectric dominates the PGBS degradation, while the oxygen vacancies control the NGBS degradation.

1. Introduction

Amorphous oxide semiconductors, such as zinc oxide, zinc–tin oxide, and indium–gallium–zinc oxide (IGZO), are of considerable interest for next-generation thin-film transistor (TFT) applications because of their excellent electrical characteristics and transparency in the visible range of the electromagnetic spectrum [1–3]. In particular, amorphous IGZO (a-IGZO) TFT device has been recognized as one of promising candidates substituting hydrogenated amorphous silicon and low-temperature polycrystalline silicon TFTs as switching/driving devices in active-matrix liquid-crystal displays and active-matrix organic light-emitting diode displays. Besides, it possesses a large mobility, a high I_{on}/I_{off} ratio, a wide band gap, a good uniformity and applicability for low temperature processing [3–5]. The low-dielectric constant SiO_2 gate dielectric results in a poor gate control over the driving current, causing large threshold voltage (V_{TH}), poor subthreshold swing (SS), and high operating voltage in the traditional Si-based TFTs [6]. Therefore, there has been a strong demand for high-dielectric constant (high-κ) materials instead of SiO_2 that is conventionally used to improve the performance of TFT devices. Recently, many researchers have proposed various high-κ film materials as an alternative gate dielectric in a-IGZO TFTs with non-hydrogen and low operation voltage [5,7–9]. Various kinds of stacked or multilayer dielectric films, such as Al_2O_3/SiN_x stack [10], Y_2O_3/HfO_2 stack [11], AlO_x–TiO_x [12], Ta_2O_5–SiO_2 [13], Ta_2O_5–Al_2O_3 [13], have been developed for IGZO TFT applications because they can allow an increase in the bandgap and the smoothness of the films, thus reducing their leakage current and improving the dielectric–semiconductor interface properties.

Rare-earth (RE) oxide film materials have attracted considerable attention because of their use in gate dielectric for TFT applications [14,15]. Among these materials, gadolinium oxide (Gd_2O_3) film is the most promising candidate of future high-κ gate-dielectric material for a-IGZO TFT devices due to its high κ value, good thermal stability, and large conduction and valence band offsets [16–18]. In our previous report, we have explored the Gd_2O_3 gate dielectric with better electrical performances in terms of low leakage current density, high breakdown voltage, and almost no hysteresis and frequency dispersion in capacitance–voltage (C–V) curves [19]. However, RE oxide films easily react with moisture to form an unstable hydroxide film on the surface [20]. To overcome this issue, the incorporation of Ti or TiO_x into RE oxide film exhibited the improved structural and electrical properties [21,22]. There have been relatively few studied of structural properties and electrical characteristics of the $GdTiO_3$ gate dielectric for a-IGZO TFTs. For practical application, it is also required for IGZO TFT device to exhibit a fine reliability, suffering from the stability phenomena know as positive gate-bias stress (PGBS) and negative gate-bias stress (NGBS). In this article, we study the structural and electrical properties of high-κ $GdTiO_3$ gate dielectric for a-IGZO TFT devices. The structural properties of the $GdTiO_3$ films were analyzed through X-ray diffraction (XRD), Auger electron spectroscopy (AES), and atomic force microscopy (AFM) techniques. The electrical characteristics of $GdTiO_3$ a-IGZO TFT devices

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were examined. Furthermore, the electrical instability of V_{TH} on these a-IGZO TFTs was investigated under both PGBS and NGBS conditions.

2. Experiment

The a-IGZO TFTs with a $GdTiO_3$ gate dielectric in this paper were fabricated on a conventional staggered bottom-gate structure. The TFT device structures were fabricated on a SiO_2/Si substrate with a 40-nm TaN gate metal deposited by sputtering at room temperature. The $GdTiO_3$ thin film (~55 nm) was then deposited as a gate dielectric through cosputtering using both Gd and Ti targets at room temperature in a mixture of Ar and O_2 (Ar:O_2 = 4:1). During the sputtering of dielectric film, the dc power density of Gd and Ti targets was 2.2 and 1.3 W/cm^2, respectively, and the chamber pressure was maintained at ~1.3×10^{-4} Pa. The deposition rate of the dielectric film was ~0.2 Å/s. Subsequently, all samples were annealed at 400 °C in O_2 ambient for 10 min to form a $GdTiO_3$ structure. The a-IGZO channel with a thickness of 20 nm was deposited by radio-frequency (RF) sputtering using an IGZO target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 in mol ratio) at room temperature. The rf power density of IGZO target was 1.3 W/cm^2 and the chamber pressure was maintained at ~1.3×10^{-4} Pa. The deposition rate of the channel layer was ~0.4 Å/s. The channel film was then annealed at 200 °C in N_2 ambient for 10 min. Finally, the source and drain electrodes (~50 nm Al) were deposited by a thermal evaporation system and patterned by photolithography and lift-off process. The channel width (W) and length (L) of the TFTs were 100 and 10 μm, respectively.

The crystalline structure of the $GdTiO_3$ film was investigated using XRD analysis. XRD analysis was performed using a Bruker-AXS D5005 diffractometer with a Cu K_α (λ = 1.542 Å) radiation. AES was used to evaluate the elemental distribution within the $GdTiO_3$ film and across the dielectric film–TaN electrode interface. AES analysis was performed using a Thermo VG Scientific Microlab 350 system. A primary electron beam energy of 10 keV and a beam current of 1 μA were used. The 3 keV Ar^+ ions were employed for depth profile measurements. The surface morphology and roughness of the films were analyzed using an NT-MDT Solver P47 (AFM). The AFM was operated in the tapping mode for imaging. The root-mean-square (R_{rms}) roughness was measured from the AFM height images. The current–voltage (I–V) characteristics of the $GdTiO_3$ a-IGZO TFT devices were measured by Agilent 4156C semiconductor parameter analyzer. The threshold voltage was determined by the normalized constant drain current method. The field-effect mobility (μ_{FE}) was determined by the maximum transconductance at constant drain voltage (V_{DS} = 5 V). The subthreshold swing is extracted at V_{DS} = 5 V from the slope of log(I_{on}) in the subthreshold region. Moreover, the I_{on}/I_{off} ratio equals to maximum current over minimum current within the measured range.

3. Results and discussion

The crystalline structure of the $GdTiO_3$ film was investigated by XRD measurement, as shown in Fig. 1. One strong intensity $GdTiO_3$ (112) and one weak intensity $GdTiO_3$ (004) reflections were found in the XRD pattern. The crystalline structure of $GdTiO_3$ film is orthorhombic. Moreover, the surface roughness of the gate dielectric plays an important role in evaluating the electrical reliability of TFT devices [23]. The AFM analysis on the morphology of the $GdTiO_3$ thin film definitely showed that sputtering method could be utilized to deposit very smooth and uniform $GdTiO_3$ film. According to the AFM measurement, the R_{rms} value of the dielectric film was 0.43 nm in the inset to Fig. 1.

The compositional dielectric film–TaN electrode integrity was evaluated using AES elemental depth profiles. The AES sputter depth profiles of the $GdTiO_3$ film–TaN electrode are shown in Fig. 2. From AES sputter depth profiles, the Gd:Ti:O atomic ratio of dielectric film is kept about 1:1:3, indicating that this dielectric is stoichiometric $GdTiO_3$. The AES depth profiles disclosed a compositional sharpness of interface with no interdiffusion of component elements between the $GdTiO_3$ film and the TaN bottom electrode. The depth profiles also demonstrated that each element component of the $GdTiO_3$ film possessed a uniform distribution from the surface of the dielectric film to the interface of the TaN bottom electrode. These data indicate that the $GdTiO_3$ film and TaN electrode maintain chemical and thermal stability at an annealing temperature of 400 °C in O_2 gas.

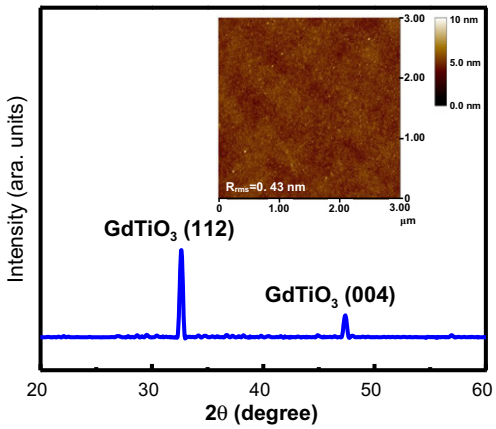

Fig. 1. XRD patterns of the $GdTiO_3$ dielectric film. Inset: AFM surface image of the $GdTiO_3$ film.

Fig. 3(a) shows the transfer characteristics of the a-IGZO TFT device featuring a $GdTiO_3$ gate dielectric. The κ value of the $GdTiO_3$ dielectric film is evaluated to be ~15 from the C–V curves. The V_{TH} of $GdTiO_3$ a-IGZO TFT device is 0.14 V, whereas the I_{on}/I_{off} ratio is 4.2×10^8. This high I_{on}/I_{off} ratio is due to the high electron mobility and low gate leakage current. The μ_{FE} of $GdTiO_3$ a-IGZO TFT device is 32.3 cm^2/V-s, while SS is 213 mV/decade. The improvement in mobility value and SS characteristics may be attributed to the smooth surface between the dielectric film and IGZO channel, resulting in the low density of interface states at the dielectric/channel interface and small amount of bulk traps in the dielectric and channel layer. On the other hand, another reason for high mobility can be attributed to the increasing gate oxide capacitance and the consequent increase in the transconductance. The inset to Fig. 3(a) depicts that the $GdTiO_3$ a-IGZO TFT device exhibited a low gate leakage current of ~10^{-12} A. The output characteristic of the $GdTiO_3$ a-IGZO TFT device is shown in Fig. 3(b). It is found that the drain current exhibits pinch-off and current saturation, indicating that such a $GdTiO_3$ a-IGZO TFT follows standard field-effect transistor characteristics.

We investigated the V_{TH} instability of $GdTiO_3$ a-IGZO TFTs under both PGBS and NGBS conditions. Fig. 4(a) and (b) displays the transfer

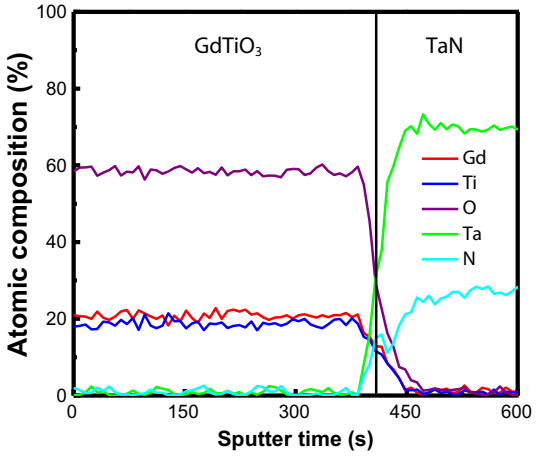

Fig. 2. Auger elemental depth profiles for $GdTiO_3$ film–TaN electrode.