Thin Solid Films 563 (2014) 6–9

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Ti–Al–O nanocrystal charge trapping memory cells fabricated by atomic layer deposition

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ARTICLE INFO

Available online 14 February 2014

Keywords:
Nanocrystal charge trapping memory
Atomic layer deposition
Band alignment

ABSTRACT

Charge trapping memory cells using Ti–Al–O (TAO) film as charge trapping layer and amorphous Al_2O_3 as the tunneling and blocking layers were fabricated on Si substrates by atomic layer deposition method. As-deposited TAO films were annealed at 700 °C, 800 °C and 900 °C for 3 min in N_2 with a rapid thermal annealing process to form nanocrystals. High-resolution transmission electron microscopy and X-ray photoelectron spectroscopy were used to characterize the microstructure and band diagram of the heterostructures. The electrical characteristics and charge storage properties of the Al_2O_3/TAO/Al_2O_3/Si stack structures were also evaluated. Compared to 700 °C and 900 °C samples, the memory cells annealed at 800 °C exhibit better memory performance with larger memory window of 4.8 V at ±6 V sweeping, higher program/erase speed and excellent endurance.

1. Introduction

The development of future flash memory requires larger storage capacity, faster program/erase speed, superior reliability for data storage, and lower energy consumption during operation [1]. However, conventional flash memory is reaching physical limits with its scaling-down dimensions [2–4]. The traditional flash memory devices using SiO_2 as tunneling layer have suffered from some issues such as the choice between high program/erase (P/E) speed and good data retention time [5]. To solve these problems, high-k materials as the tunneling layer can provide lower tunnel barriers and smaller equivalent oxide thickness [6]. The devices with high-k nanocrystals as the charge trapping layer are also getting much attention. Compared with the conventional charge trapping layers, high-k dielectric films allow a higher electric field over the tunneling layer because of electric flux density continuity [7], thus improving P/E speed. Besides, high-k materials as blocking layer, such as Al_2O_3 film, can enhance the device performance like lower P/E voltage and scaling ability. In this paper, we reported a charge trapping memory cell with Al_2O_3 film as tunneling layer and blocking layer and Ti–Al–O nanocrystals as the charge trapping layer prepared by atomic layer deposition (ALD) [8–10].

2. Experiment details

P-type (100) Si wafers were cleaned by the standard Radio Corporation of America (RCA) process. Then the native oxide layers were removed by dipping the wafers in dilute HF solution for 2 min. Then the wafer was transferred to an ALD reactor (Picosun SUNALE R 150B). A thin tunneling Al_2O_3 layer of 40 cycles, Ti-doped Al_2O_3 layer as the charge trapping layer (24 cycles of Ti source and 16 cycles of Al source as a sequence for 3 periods, total 120 cycles), and Al_2O_3 of 120 cycles as the blocking layer at 250 °C were deposited using $Al(CH_3)_3$, $Ti(O\text{-}i\text{-}Pr)_4$ as metal sources and H_2O as oxygen source. Subsequently, the above memory cells were rapid thermally annealed at 700 °C, 800 °C or 900 °C for 3 min in N_2 ambient. Finally, Pt top electrodes with an area of 1.53×10^{-4} cm^2 were deposited by sputtering method at room temperature and Ag paste was spread on the back side of p-Si substrate as the bottom electrodes.

The electrical properties of the Al_2O_3/TAO/Al_2O_3/Si stack structures were measured at 1 MHz using Keithley 4200 semiconductor characterization system. In order to characterize the band diagram of the stack structures, the samples were analyzed via X-ray photoelectron spectroscopy (XPS, Thermo Fisher K-Alpha) with a monochromatic Al Kα source ($h\nu = 1486.6$ eV) for excitation of photoelectrons. A high-resolution transmission electron microscope (HRTEM) (Tecnai F20) was used to characterize the microstructure of the memory cells.

3. Results and discussion

Fig. 1(a) and (b) show the cross-sectional HRTEM images of the memory cells annealed at 800 °C and 900 °C for 3 min, respectively. In Fig. 1(a), after annealing at 800 °C, the interfaces between p-Si and Al_2O_3, Al_2O_3 and TAO, and TAO and Al_2O_3 are distinct and sharp with thickness of the Al_2O_3/TAO/Al_2O_3/Si stack of 11.7 nm/10.4 nm/2.9 nm. In Fig. 1(b), the higher annealing temperature of 900 °C leads to evident interdiffusion and the interface between charge trapping layers of TAO

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http://dx.doi.org/10.1016/j.tsf.2014.02.024
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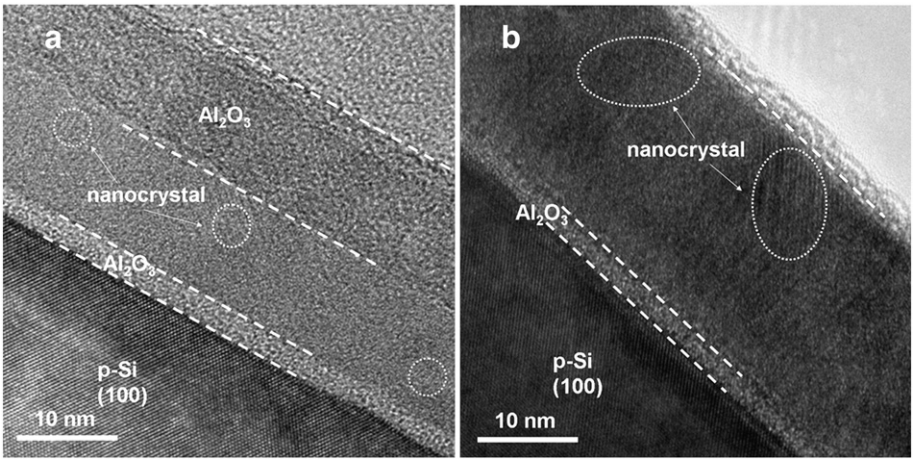

Fig. 1. HRTEM cross-sectional images of the memory cells annealed at (a) 800 °C and (b) 900 °C.

and blocking layer of Al_2O_3 cannot be recognized. The thickness of tunneling oxide becomes thinner (~2.3 nm). After 800 °C annealing, spherical nanocrystals are observed in the charge storage layer of TAO films with the average size of 3 nm, as marked in Fig. 1(a). Meanwhile, Al_2O_3 films as the tunneling and blocking oxide layer still keep amorphous features. These nanocrystals embedded in the TAO layer will play a key role in capturing electrons for memory behavior. 900 °C annealing produces larger ellipsoidal nanocrystals of ~10 nm in Fig. 1(b).

To better understand the working mechanism of the Al_2O_3/TAO/Al_2O_3/Si stack, the band alignment of the heterostructure annealed at 800 °C was determined by measuring the valence band offsets (VBOs) and O *1s* electron energy loss spectra by XPS [11]. The VBO values are obtained based on the assumption that the energy difference between the core level and the valence band edge of the substrate remains constant with/without the film deposition. Here, Si *2p* spectrum is chosen as the reference to determine the VBO [12]. The valence band maximum (VBM) of p-Si substrate is determined as 0.43 eV (E_{VBM}^{Si}) by using the linear extrapolation. The VBM at the interface of Al_2O_3/Si, TAO/Al_2O_3, and Al_2O_3/TAO is determined as 3.06 eV $\left(E_{VBM}^{Al_2O_3}\right)$, 2.47 eV ($E_{VBM}^{TAO}$) and 2.96 eV $\left(E_{VBM}^{Al_2O_3}\right)$ respectively, as shown in Fig. 2(a). Consequently, the VBO of Al_2O_3/Si $\left(\Delta E_v^{Al_2O_3/Si}\right)$ is calculated as 2.63 eV by using Eq. (1). So the VBO of TAO/Al_2O_3 and Al_2O_3/TAO is determined to be −0.59 eV and 0.49 eV, respectively. The bandgap of Al_2O_3, TAO and Al_2O_3 is determined to be 7.49 eV, 5.41 eV and 7.05 eV, respectively, by the onsets of O 1s electron energy loss spectra at the interface of TAO/Al_2O_3 and Al_2O_3/TAO as seen in Fig. 2(b). The thinner Al_2O_3 tunneling layer (~2.9 nm) has a wider bandgap than the thicker Al_2O_3 blocking layer (~11.7 nm). It is related to the formation of interfacial layer of $AlSi_xO_y$ between Si substrate and ultrathin Al_2O_3 tunnel oxide after 800 °C annealing. Evidently the bandgap of $AlSi_xO_y$ is wider than the pure Al_2O_3.

The conduction band offset (CBO) of Al_2O_3/Si $\left(\Delta E_c^{Al_2O_3/Si}\right)$ can be calculated as 3.74 eV by using Eq. (2), where E_g^{Si} is 1.12 eV. Then the CBO of TAO/Al_2O_3 and Al_2O_3/TAO is estimated to be 1.49 eV and 1.15 eV, respectively. The work function of Pt is 5.65 eV [13] and the electron affinity of Si substrate is 4.05 eV [14].

$$\Delta E_v^{Al_2O_3/Si} = E_{VBM}^{Al_2O_3} - E_{VBM}^{Si} \quad (1)$$

$$\Delta E_c^{Al_2O_3/Si} = E_g^{Al_2O_3} - E_g^{Si} - E_v^{Al_2O_3/Si} \quad (2)$$

The band diagram of the heterostructure is schematically drawn in Fig. 3 based on these results. The data retention characteristics are associated with the temperature, the tunneling layer thickness, the CBOs, and trap energy levels. In Fig. 3, the large CBO between TAO and Al_2O_3 will enhance the retention characteristics due to the deep trap level. Meanwhile, the deep trap level between TAO and Al_2O_3 can suppress the migration of trapped electrons in the TAO nanocrystal charge trap memory cells. On the other hand, the lateral migration of electrons trapped in TAO nanocrystals may be hindered due to effective separation by the amorphous Al_2O_3 matrix.

Fig. 4(a) plots the capacitance–voltage (C–V) curves of the Al_2O_3/TAO/Al_2O_3/Si stack structures annealed at 700 °C, 800 °C and 900 °C. The behavior of the memory cells was measured by scanning from 6 V

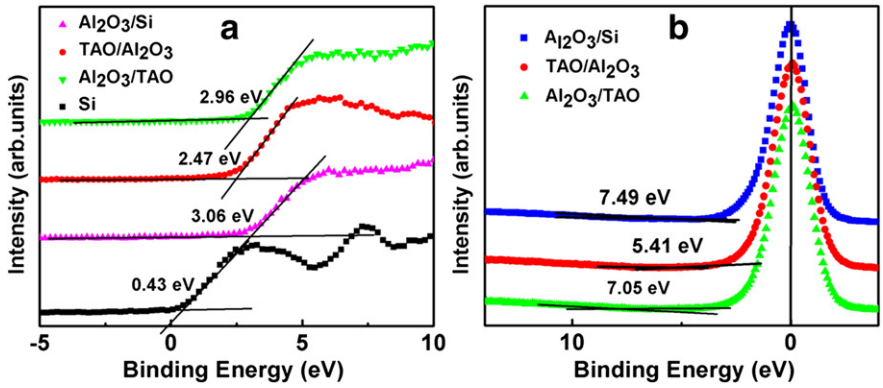

Fig. 2. (a) The valence band spectra of the p-Si substrate, Al_2O_3/p-Si, and TAO/Al_2O_3 and (b) O 1s electron energy loss spectra of TAO/Al_2O_3 and Al_2O_3/TAO. The memory cell was annealed at 800 °C.