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The effect of Al_2O_3 passivation layer in pulsed-laser-deposited ZrO_2 films on n-GaAs substrate as a function of post-annealing temperature

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ABSTRACT

We investigated the thermal stability of ZrO_2/GaAs structures deposited by pulsed laser deposition as a function of the post-annealing temperature. During the annealing process the interfacial layer between the pulsed laser deposited ZrO_2 thin film and GaAs substrate increased significantly at the temperature of 500 °C, and the ZrO_2 thin film became fully crystallized to the monoclinic phase at the temperature of 600 °C. This resulted in the degradation of electrical properties such as the leakage current and the breakdown voltage, and an interfacial trap charge density. In order to improve the thermal stability, we pre-deposited an Al_2O_3 passivation layer by atomic layer deposition followed by pulsed laser deposited ZrO_2 deposition. The amorphous Al_2O_3 passivation layer hindered the crystallization of the ZrO_2 thin film during the annealing process, significantly improving the electrical characteristics of the resulting structure compared to the ZrO_2/GaAs structures without an Al_2O_3 passivation layer. In particular, the interfacial reaction was effectively suppressed up to a temperature of 600 °C so that the interface trap charge density was significantly decreased due to the low oxygen diffusivity of Al_2O_3 layer.

1. Introduction

Ultimate scaling down of Si metal-oxide-semiconductor (MOS) transistors faces too many challenges, such as an increase in leakage current by direct tunneling of electrons, power consumption, and high operating speed [1–3]. To address these challenges, many channel materials and gate dielectric materials are currently being investigated by several research groups. III–V compound semiconductors, such as GaAs, InP, and InGaAs are receiving enormous attention as probable channel materials. Among those semiconductors, GaAs is applicable to n-type high-speed devices due to its high electron mobility (8500 $cm^2\ V^{-1}\ s^{-1}$) and low power consumption. However, GaAs-based MOS devices lack stability and high quality native oxides in comparison to SiO_2 on Si. Therefore, numerous efforts have been made to find promising gate dielectric material with a large bandgap and a high dielectric constant (high-k) to reduce leakage current and obtain a high capacitance. Among these high-k materials, ZrO_2 is one of the most attractive candidates due to its high-k value (~25) and large bandgap (5.8 eV) [4].

The thermal instability of the interface between GaAs substrate and various gate oxides such as HfO_2, Al_2O_3, Y_2O_3, TiO_2, etc. has been reported [5–8]. Reported data shows that Ga oxides or As oxides formed during the thermal process induce a high density of interface charge traps that cause Fermi level pinning [9,10]. Several studies have used a surface treatment to reduce the interfacial charge traps before oxide film deposition. An ammonium sulfide was treated on GaAs substrate before the deposition of TiO_2 film to decrease interface defects effectively [8,11]. Nitridation is also expected to help decrease interfacial defects by a curing process [12–14]. In the present, insulting the passivation layer between the high-k film and the substrate has been suggested to improve thermal stability and adjust the proper band offset. Si is one of proposed materials for the passivation layer, because Si-interfacial passivation layer can reduce the interface state density and prevent Fermi level pinning at the interface between GaAs and a high-k oxide film by suppressing thermal oxidation due to Si–As bonding during the thermal process [15–18]. On the other hand, oxide films have been also suggested for passivation layers to prevent thermal oxidation due to residual oxygen that diffuses into the interface through the high-k film during the thermal process. Some researchers have proposed that Al_2O_3 film, which has low diffusivity and remarkable thermal stability, be pre-deposited before high-k film deposition to reduce interfacial defects, while other authors have suggested post-deposition of oxide film to cap the high-k film from the diffusion of residual oxygen during the thermal process [19–22]. Al_2O_3 passivation or capping layer is deposited mainly by atomic layer deposition (ALD). ALD process facilitates the deposition of uniformly ultrathin oxide film with a clean interface and low defect levels.

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There are several reports for ZrO_2/GaAs system deposited using various methods. Dalapati et al. investigated the interfacial characteristics and electrical characteristics of a sputtered ZrO_2 gate dielectric on a p-GaAs substrate and showed that a Si-passivation layer improved the interface quality [23]. Kundu et al. also studied on the ZrO_2/GaAs system deposited by the sol–gel process and its interface engineering with a ZnO interface passivation layer [24,25]. In this paper, we investigated the thermal stability of ZrO_2/GaAs deposited by pulsed laser deposition (PLD) process as a function of annealing temperature. We focused on the structural and chemical bonding properties of ZrO_2 film and the interfacial reaction between ZrO_2 and GaAs substrate. In addition, to improve interfacial characteristics, we investigated the effect of the interfacial passivation layer deposited by atomic layer deposition before ZrO_2 deposition as a function of the post-annealing temperature. Improved interfacial characteristics afforded by the interfacial passivation layer were also verified by electrical measurements. Conducting process of charge carriers and the distribution of defects were investigated by using metal oxide semiconductor capacitor structure with TiN electrode.

2. Experimental details

We used N-type GaAs (100) (Si-doped with concentration of 1×10^{18} cm^{-3}) wafer as a substrate. After immersing the substrate in a buffed oxide etchant (NH_4F: HF = 6:1) solution for 1 min and rinsing with deionized water, ZrO_2 thin film was deposited with a PLD system. During the deposition process, the substrate was heated to a temperature of 200 °C and the O_2 pressure was maintained at 0.667 Pa. An Al_2O_3 interfacial passivation layer was deposited at the substrate temperature of 270 °C using ALD with trimethylaluminium and deionized water precursors. Post-deposition annealing (PDA) process was conducted by rapid thermal annealing (RTA) at 500 °C and 600 °C for 1 min under N_2 (99.9999%) ambient. A MOS capacitor structure was produced by fabricating a TiN electrode using the lift-off method. The deposited TiN electrode was a square with a length of 80 μm and a thickness of 120 nm.

Changes in structural properties of PLD-ZrO_2/GaAs and PLD-ZrO_2/ALD-Al_2O_3/GaAs as a function of annealing temperature were investigated by high-resolution transmission electron microscopy (HR-TEM) with fast Fourier transformation (FFT) images (JEM-2100F) at an accelerating voltage of 200 keV. X-ray diffraction (XRD) patterns were taken by a θ/2θ scan with a monochromatic Cu Kα radiation source and a wavelength of 0.15418 nm. The chemical structure of the film and interface between the oxides and the substrate were investigated by high-resolution X-ray photoelectron spectroscopy (HR-XPS) with monochromatic Al Kα source (1486.6 eV) run at 15 kV and 1.67 mA varying the take-off angle. The higher the take-off angle, the deeper is the effective sampling depth in XPS spectra [26,27]. XPS spectra were compensated with C1s bonding energy of 285 eV. We fitted all XPS spectra with mixed Lorentzian–Gaussian curves and a Shirley background by using Fitt-win software. The full width at half maximum (FWHM) of the Lorentzian peaks was assumed to be the same for each curve to 0.1 eV. The FWHM for Gaussian peaks was 0.9–1.2 eV and was similar for each curve. Electrical properties of films, such as voltage breakdown and capacitance value, were obtained by measuring current–voltage (J–V) curves by using Model 2400 SourceMeter of Keithley Instruments Inc. and capacitance–voltage (C–V) curves at 100 kHz using E4980A Precision LCR meter of Agilent Technologies, Inc. To verify the decrease of defect states, conductance measurements were performed in the frequency range of 1 kHz to 1 MHz using the same LCR meter [28].

3. Results and discussion

We obtained HR-TEM images to investigate the structural changes after the annealing process of ZrO_2/GaAs without an Al_2O_3 passivation layer. Cross-sectional HR-TEM micrographs of (a) as-grown and samples post-annealed at (b) 500 °C and (c) 600 °C are shown in Fig. 1. The deposited ZrO_2 thin films on the GaAs (100) substrate had a uniform thickness of 4 nm. An abrupt interface without any interfacial layer was observed in the as-grown samples, while the thickness of the interfacial layer increased enormously during the PDA process: the thicknesses of the interfacial layers at the annealing temperatures of 500 °C and 600 °C were 8.5 nm and 9.5 nm, respectively. These thick interfacial layers have not been reported using other deposition techniques such as the sputtering method or the sol–gel process [23,25]. The thickness of this layer is likely due to the fast diffusion of oxygen atoms through the crystalline ZrO_2 films and the residual oxygen incorporated in the interface by ambient O_2 during the PLD process. The inset in Fig. 1(c) is the FFT image of the ZrO_2 film after the PDA process at 600 °C. Although we could only acquire the clear FFT image of the sample that underwent PDA temperature of 600 °C, the crystallized structure of ZrO_2 was partially found in all samples. The structure of the crystallized ZrO_2 thin film based on the analysis of the diffraction pattern is consistent with a monoclinic crystal structure (a =0.5142 nm, b = 0.52 nm, c = 0.5311 nm, and β = 97°) [29]. Additionally, the crystalline structure was examined by XRD (Fig. 1(d)) and we obtained three peaks at 24.89°, 32.28°, and 43.87°, representing the ZrO_2 (110), (111), and (−112) directions of monoclinic phase, respectively. These results indicate that the ZrO_2 film in the ZrO_2/GaAs structures gradually crystallized to a fully monoclinic phase at the temperature of 600 °C. TEM images of the ZrO_2 film of the as-

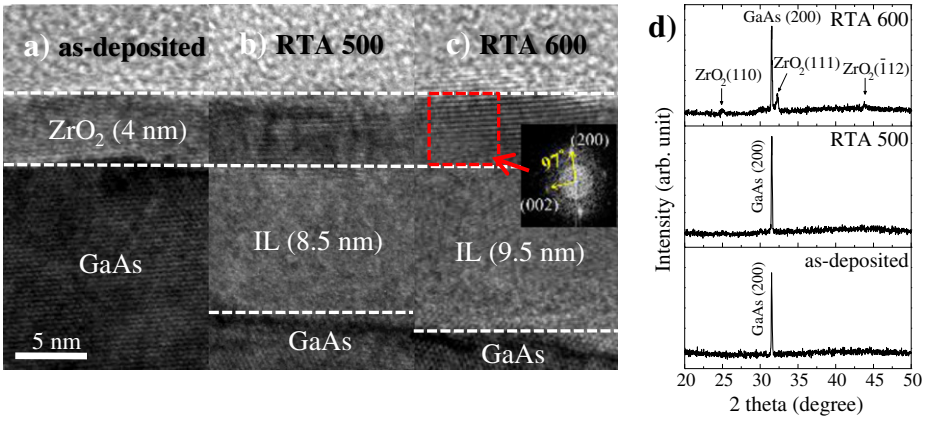

Fig. 1. (a)–(c). Cross-sectional HR-TEM photographs of PLD-ZrO_2/GaAs structures as a function of the annealing temperature. Inset of (c) is a FFT image of ZrO_2 thin films. (d). X-ray diffraction patterns to show the crystalline structure of ZrO_2.