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Electrical transport mechanisms in amorphous/crystalline silicon heterojunction: Impact of passivation layer thickness

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ABSTRACT

We investigate the current transport mechanisms in the amorphous silicon/crystalline silicon heterojunction and the change of these processes when an intrinsic amorphous silicon passivation layer with a varying thickness is introduced at the interface. We present analyses of temperature dependent dark current–voltage curves, which allow determining the prevalent current transport path in heterojunction structures. It is shown that the intrinsic passivation layer plays an important role in the current transport in the heterojunction and the thickness of such an interlayer has to be considered when such structures are analyzed.

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1. Introduction

The opportunity to achieve a high performance and still maintain low fabrication costs makes the heterojunction with intrinsic thin layer solar cells (HIT) attractive for many research groups [1–3]. The physical processes of charge transport through the amorphous silicon/crystalline silicon (a-Si:H/c-Si) interface, as well as band alignment at the heterojunction have a crucial influence on the solar cell performance. A thin intrinsic layer of amorphous silicon is usually introduced between the doped amorphous and crystalline silicon layers to passivate the interface and hereby to achieve the high performance. Although the industrial fabrication of HIT solar cells is already well established by company Panasonic, fundamental questions concerning the passivation effect of the intrinsic layer and the current paths in the heterojunction still need to be studied in detail.

The first work with an attempt to describe the processes at the a-Si:H/c-Si heterojunction dates back to 1975 [4]. Since then, various studies have shown the dominating recombination in the space charge region [5,6] and the neutral part of the semiconductor [7], or the prevalence of tunneling process [8]. The comprehensive study published by Schulze et al. [9] points at a direct link between the dominant current transport mechanism and the output performance of the solar cell. In this study the state-of-the-art solar cells with the interface passivated by an intrinsic amorphous silicon layer exhibited the prevalence of the tunneling transport mechanism in the low voltage region of forward biased current–voltage (*I*–*V*) characteristics. While the interface condition clearly affects the current transport, the open question under dispute is the impact of the passivation layer thickness on the current transport mechanism. One of the first investigations of this issue was done by Page et al. [10] for a-Si:H(p)/c-Si(n) heterojunction solar cell structure. For this doping sequence the field drift transport of holes was observed as a dominating current path regardless of the passivation layer thicknesses. However, there is a lack of similar studies for structures with a-Si:H(n)/c-Si(p) doping. The aim of this paper is to study the influence of the intrinsic passivation layer on the transport mechanism in structures with an a-Si:H(n)/c-Si(p) heterojunction. Attention is focused on the impact of the passivation layer thickness on the charge carrier transport. The investigation was provided using the analysis of dark current–voltage curves measured at different temperatures, which has been established as a standard method to determine the dominant physical phenomena of carrier transport.

2. Fabrication and experimental details

Analysis of the current transport through the intrinsic passivation layer was conducted on the a-Si:H(n)/c-Si(p) heterojunction structures. Two series of a-Si:H(n)/c-Si(p) samples with 5 nm and 10 nm thick a-Si:H(i) passivation layers and one reference sample without the passivation layer were prepared in the Laboratory of Photovoltaic Materials and Devices, TU Delft in the Netherlands. In the text, the samples are referred as A5, A10 and A0, for structures with 5 nm and 10 nm thick

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intrinsic passivation layers and for the structure without passivation layer, respectively. The thickness of the phosphorous doped amorphous silicon layer is 50 nm for all samples. Polished p-type silicon wafers with <111> orientation are used as a substrate. The wafer thickness is 525 μm. The exact resistivity was measured by 4-point probe and has a value of 8 Ω cm, which corresponds to doping concentration 1.6×10^{15} cm^{-3} [11]. After deposition of amorphous silicon was further processing and measuring of the samples carried out in the Institute of Electronics and Photonics, Faculty of Electrical Engineering and Information Technology, Slovak University of Technology in Bratislava. Top aluminum circle electrodes with a diameter of 500 μm were defined by a "shadow mask" and full area bottom electrodes are evaporated to form a heterojunction diode. To suppress the high lateral leakage current, the samples were patterned by MESA reaction ion etching of a-Si:H (n) and a-Si:H(i) layers. High etching selectivity of the silicon compared to metal (600:1) allowed aluminum gates to be used as a mask. The aim of the study is the comparison of current transport mechanisms in structures with different thicknesses of intrinsic passivation layer. Thus equal MESA processes were conducted for all samples to assure similar conditions regarding the recombination contribution from the exposed flanks across the junction. Current–voltage measurements were conducted in a setup of Keithley 237. Temperature dependent *I–V* measurements are made in the range 303 to 403 K with a step of 10 K.

3. Results and discussion

Various physical phenomena are involved in the current transport through the heterojunction. Usually, one of them predominates and can be specified by monitoring the temperature dependence of current–voltage characteristics. In general, the *I–V* curve is described using the well-known formula

$$J = J_0[\exp(AV) - 1] \tag{1}$$

where J_0 denotes the saturation current density and A represents the temperature dependent exponential factor defined as $A = q/nkT$, where n is the diode ideality factor. Every mechanism of current transport is characterized by its particular temperature expression of the exponential factor A. If the current has a tunneling nature, parameter A has a weak or no dependence upon the temperature. For the recombination type of current, parameter A changes with temperature. The basic information concerning the source of recombination is obtained by the value of the diode ideality factor n. Recombination through the states at the interface or in the neutral part of the semiconductor is characterized by a diode ideality factor close to 1 [12]. In the case of recombination in the space charge region, the diode ideality factor is equal to 2 in an ideal case of one recombination level lying at the midgap and with an identical capture cross sections for electrons and holes. Due to a continuous distribution of defect states in amorphous silicon the recombination takes place through various trap levels and the diode ideality factor lies between 1 and 2 [13,5]. The source of recombination can be more clearly identified by analyzing the Arrhenius plot of the saturation current. The temperature dependence of the saturation current is given by

$$J_0 \approx \exp\left(\frac{-E_{ac}}{kT}\right), \tag{2}$$

where T is temperature and k is the Boltzmann constant. Activation energy E_{ac} obtained from such an Arrhenius plot identifies the prevalent current transport process in the structure. Recombination in the neutral part of the semiconductor has E_{ac} equal to the band gap of the semiconductor, in which this recombination takes place. While the recombination in the space charge region is dominated by the states near the midgap, the activation energy of the saturation current has a value close to one half of the semiconductor band gap. Recombination at the a-Si:H(n)/c-Si(p) interface is characterized by an activation energy equal to the effective barrier height [12]

$$\varphi_b = qV_D + E_a^{c\text{-}Si}, \tag{3}$$

where V_D is the diffusion voltage in the heterostructure and E_a^{c-Si} denotes the energy difference between the bulk Fermi level E_F and the valence band level E_V of crystalline silicon. The schematic drawn of a-Si:H(n)/c-Si(p) heterojunction with depicted barrier for interface recombination (φ_b) is shown in Fig. 1. It is important to notice that the overall diffusion voltage in the sample has two components, diffusion voltage distributed in the amorphous silicon $V_D^{a\text{-}Si:H}$ and in the crystalline silicon $V_D^{c\text{-}Si}$. For heterojunction with donor doping concentration in the emitter significantly higher compared to acceptor concentration in the crystalline silicon, almost the whole diffusion potential is distributed in the crystalline silicon substrate and with good approximation we can write $V_D \cong V_D^{c\text{-}Si}$.

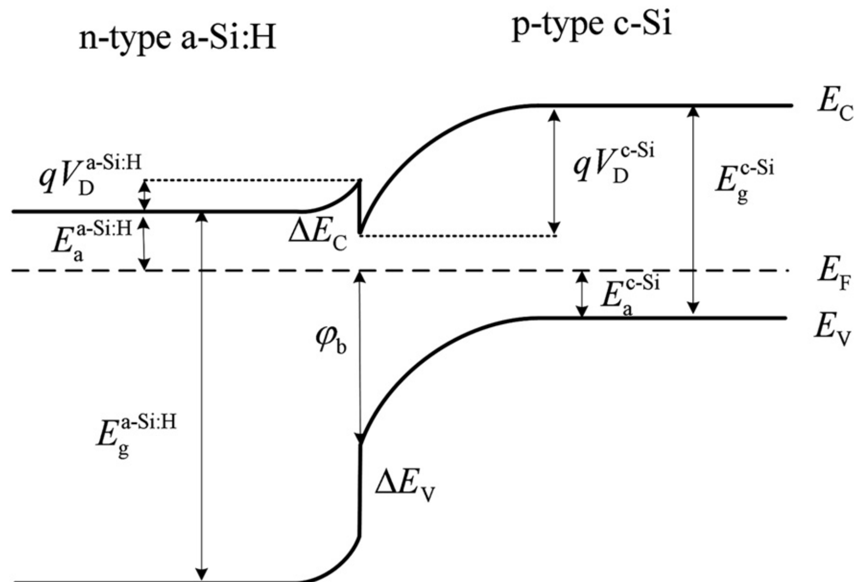

Fig. 1. Band diagram of the a-Si:H(n)/c-Si(p) heterojunction. The parameter φ_b represents barrier for recombination through the defect states at the interface.

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