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Self-aligned top-gate InGaZnO thin film transistors using SiO_2/Al_2O_3 stack gate dielectric

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ABSTRACT

Self-aligned top-gate amorphous indium–gallium–zinc oxide (a-IGZO) thin film transistors (TFTs) utilizing SiO_2/Al_2O_3 stack thin films as gate dielectric are developed in this paper. Due to high quality of the high-k Al_2O_3 and good interface between active layer and gate dielectric, the resulting a-IGZO TFT exhibits good electrical performance including field-effect mobility of 9 cm^2/Vs, threshold voltage of 2.2 V, subthreshold swing of 0.2 V/decade, and on/off current ratio of 1×10^7. With scaling down of the channel length, good characteristics are also obtained with a small shift of the threshold voltage and no degradation of subthreshold swing.

1. Introduction

Recently, amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs) have become attractive for use as driving devices in large scale active matrix organic light emitting diode (AMOLED) display applications, due to their higher mobility and larger area uniformity, as compared to amorphous silicon (a-Si) and polycrystalline silicon (p-Si) TFTs [1–5]. The conventional a-Si TFTs, which are used as switching devices in active matrix liquid crystal display, have the advantages of low manufacturing cost and large area uniformity. However, their low field-effect mobility (<1 cm^2/Vs) may be not sufficient to drive AMOLED. Due to their high mobility (>50 cm^2/Vs) and electrical stability, the conventional p-Si TFTs are currently used as driving devices in AMOLED displays. But the main issues are the non-uniformity of their field-effect mobility and threshold voltage, caused by the grain size and grain boundaries in p-Si thin films.

Conventional bottom-gate structure is widely studied for a-IGZO TFTs. But this structure is unsuitable for the integration of peripheral circuits for the system on glass and realization of high resolution high quality AMOLED displays, due to the high parasitic capacitance and poor scalability. Therefore, the development of self-aligned top-gate a-IGZO TFTs with good electrical performance is necessary.

A number of gate dielectrics have been investigated for ZnO-based TFTs, such as HfO_2 [6], SiO_2 [7], Si_3N_4 [8], Y_2O_3 [1], and Al_2O_3 [4,9]. Due to the high relative permittivity of ~9 and good thin film quality, Al_2O_3 deposited by atomic layer deposition (ALD) is a promising gate dielectric material for oxide TFTs. However, it shows poor interface between the a-IGZO semiconductor and Al_2O_3 thin film, because the ALD deposition process contains water vapor. In this paper, SiO_2 thin film deposited by plasma enhanced chemical vapor deposition (PECVD) is utilized as a buffer and protective layer between a-IGZO semiconductor and Al_2O_3 thin film. The resulting self-aligned top-gate a-IGZO TFTs with SiO_2/Al_2O_3 stack gate dielectric exhibits a field effect mobility of 9 cm^2/Vs, a threshold voltage of 2.2 V, a subthreshold swing of 0.2 V/decade and an on/off current ratio of 1×10^7.

2. Experimental details

The cross-sectional schematic of the self-aligned top-gate type a-IGZO TFT studied in this paper is shown in Fig. 1.

A 100 nm thick a-IGZO active layer was first sputtered on thermally oxidized silicon wafer with the oxide thickness of 500 nm by DC magnetron sputtering using a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol% in a mixed argon and oxygen ambient at room temperature. The gas flow ratio between argon and oxygen is 18:7. The deposition pressure and the power were 0.26 Pa and 120 W, respectively. After patterning this a-IGZO active layer by lift-off process, a 15 nm thick SiO_2 layer as buffer and protective layer was deposited by PECVD on top of the a-IGZO layer at 300 °C. Then, a 15 nm think Al_2O_3 layer as gate dielectric was deposited by ALD at 300 °C. The SiO_2 layer acted as a protective layer for a-IGZO thin film during the ALD process, which contains water vapor. After that, a 100 nm thick indium tin oxide (ITO), used as gate electrode, was sequentially sputtered at room temperature, and then defined using photolithography and lift-off process. Then, annealing process was executed at 200 °C for 30 min in a N_2 and O_2 ambient. By reactive ion etching, the SiO_2/Al_2O_3 gate dielectric was then self-aligned dry etched using ITO gate electrode pattern as a mask. After that, SiO_2 layers were deposited as passivation layers by PECVD

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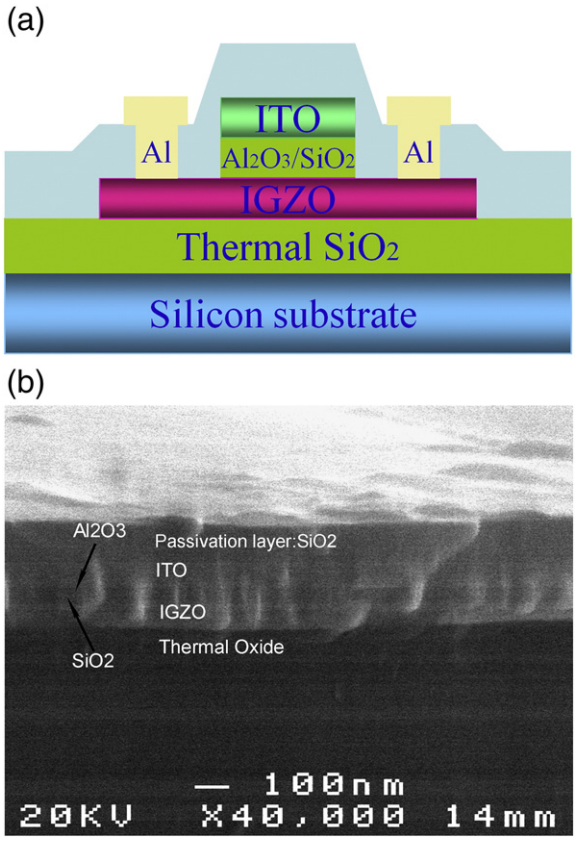

Fig. 1. (a) Cross-section schematic of the proposed a-IGZO TFT with self-aligned top-gate structure and (b) SEM cross-section image of the a-IGZO TFT.

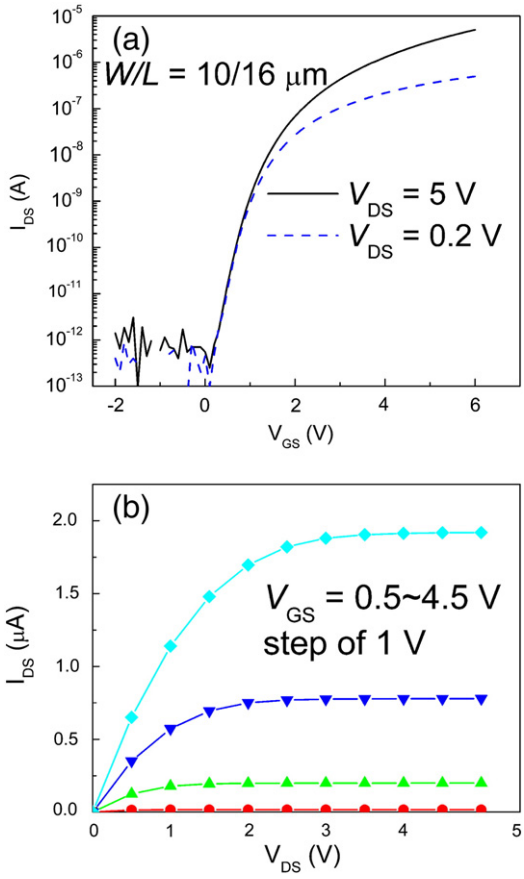

Fig. 2. (a) Transfer and (b) output characteristics of the fabricated a-IGZO TFTs with SiO_2/Al_2O_3 gate.

at 150 °C. After forming the contact holes, a 200 nm thick Al layer was deposited by sputtering and patterned as gate/source/drain electrodes. The electrical properties of the a-IGZO TFTs were measured using an HP4156A precision semiconductor parameter analyzer. The substrate is grounded during the electrical characterization.

3. Results and discussion

The field effect mobility induced by the transconductance at a low drain voltage is given by

$$\mu_{FE} = \frac{Lg_m}{WC_{OX}V_{DS}} \quad (1)$$

where g_m and C_{OX} are the transconductance and the gate dielectric capacitance per unit area, respectively. Fig. 2 shows the typical transfer and output characteristics of the fabricated a-IGZO TFTs with a width to length ratio of 10/16 μm. They exhibit good transfer TFT characteristics at V_{DS} of 0.2 V such as a field effect mobility of 9 cm^2/Vs, a threshold voltage of 2.2 V, a subthreshold swing of 0.2 V/decade and an on/off current ratio of 1×10^7. The saturate mobility of about 8.1 cm^2/Vs is also obtained at a $V_{DS} = 5$ V. The linear mobility and saturate mobility obtained are nearly comparable, implying that the field effect mobility is independent on drain voltage. The output characteristic shows clear linear regions and does not show significant current crowding at low V_{DS}, indicating that low series resistance in source/drain contacts was obtained.

Fig. 3(a) shows the dependence of the channel length (L) on the field-effect mobility of the a-IGZO TFTs with the channel width of 30 μm. As the channel length decreased from 16 μm to 2 μm, the maximum field-effect mobility of the a-IGZO TFTs decreased from 9 to 3.9 cm^2/Vs. The decrease of the field-effect mobility for short channel devices is due to the existence of the source/drain series resistance R_{SD} on the potential distribution across the channel. Without considering this effect of R_{SD}, the field-effect mobility extracted using Eq. (1) underestimates the true field-effect mobility for the a-IGZO TFTs. In order to obtain the true field-effect mobility, the R_{SD} could be extracted by using the following relationship [10]:

$$\mu_{FE} \approx \mu_0 \frac{L}{L + \mu_0 W C_{OX} R_{SD}(V_{GS} - V_{th})} \quad (2)$$

where μ_{FE} is the apparent field-effect mobility and μ_0 is the true field-effect mobility of the a-IGZO material. The R_{SD} for the a-IGZO TFTs was extracted to be 24 kΩ from the fitting of the apparent field-effect mobility in Fig. 3(b) using Eq. (2). The width-normalized $R_{SD}W$ was 72 Ω cm. As a result, the true channel mobility was extracted to be 11.2 cm^2/Vs for the a-IGZO TFTs.

The R_{SD} was also extracted by determining the device on-resistance R_{on} from the linear region of the transfer characteristics and plotting the width normalized $R_{on}W$ as a function of the L for different gate voltages [11]. Fig. 4 shows the width normalized $R_{on}W$ as a function of L at different gate voltages at $V_{DS} = 0.2$ V for the a-IGZO TFTs. The $R_{SD}W$ for the a-IGZO TFTs, which is extracted at the y-axis intercept of the extrapolated linear fit of $R_{on}W$ versus L, is approximately 60 Ω cm for $V_{GS} = 6$ V, which is similar to that of bottom-gate a-IGZO TFTs [3]. The $R_{SD}W$ value extracted by this method is similar to that extracted from the fitting result in Fig. 3(b) using Eq. (2). This low source/drain series resistance is caused by the hydrogen diffusion into source/drain areas during over-etch of the gate dielectric SiO_2/Al_2O_3 dry-etching process with CHF_3/O_2 plasma. Hydrogen diffusion into the a-IGZO thin film can cause low resistivity of the a-IGZO. Hydrogen is an n-type dopant for a-IGZO thin film [12,13]. The carrier concentration of the a-IGZO is estimated to be 3×10^{19} cm^{-3}.