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Fabrication of enhancement-mode AlGaN/GaN high electron mobility transistors using double plasma treatment

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ABSTRACT

We report the fabrication and DC and microwave characteristics of 0.5 μm AlGaN/GaN high electron mobility transistors using double plasma treatment process. Silicon nitride layers 700 and 150 Å thick were deposited by plasma-enhanced chemical vapor deposition at 260 °C to protect the device and to define the gate footprint. The double plasma process was carried out by two different etching techniques to obtain enhancement-mode AlGaN/GaN high electron mobility transistors with 0.5 μm gate lengths. The enhancement-mode AlGaN/GaN high electron mobility transistor was prepared in parallel to the depletion-mode AlGaN/GaN high electron mobility transistor device on one wafer. Completed double plasma treated 0.5 μm AlGaN/GaN high electron mobility transistor devices fabricated by dry etching exhibited a peak transconductance, gm, of 330 mS/mm, a breakdown voltage of 115 V, a current-gain cutoff frequency (f_T) of 18 GHz, and a maximum oscillation frequency (f_{max}) of 66 GHz.

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1. Introduction

As a promising candidate for next generation power device materials, GaN have attracted much research interest due to the inherent advantages of a high critical electric field and a high electron mobility compared to those of Si. In particular, AlGaN/GaN high electron mobility transistor (HEMT) is a promising power device because it has a high voltage and high power density. For power electronics applications, enhancement-mode (E-mode) operation is strongly required to simplify the design of driving circuits. However, it is difficult to obtain E-mode operation with a low on-state resistance and a high breakdown voltage. Recently, some groups have demonstrated enhancement-mode GaN-based electric devices [1]. Several technologies for the enhancement-mode operation of the AlGaN/GaN HEMTs have been reported such as using a thin AlGaN barrier layer [2–4], a recessed gate structure [5,6], and using a fluoride-based plasma treatment [7,8]. One technique to increase the transconductance is to minimize the distance from the gate to the active channel of the transistor by etching a gate recess. Often a gate recess process is required to etch away a highly doped contact layer which is grown on the upper AlGaN layer to increase field induced band shift. This gate recess process is one of the most critical steps in the fabrication of recessed AlGaN/GaN HEMTs because it determines the threshold voltage and the gate leakage current of the device. Therefore, the accurate control of the recess etching depth is required for realization of the normally-off operation. However, these recessed devices have very low threshold voltage and large gate leakage current. The key processing step is to produce low damage gate-recess etching of AlGaN. For the gate recess step during device fabrication, the inertness of GaN materials to chemicals dictates the use of dry etching techniques which involve energetic particles. The use of plasma may create surface damage leading to increase in gate leakage and the creation of traps which may limit the performance of the devices. The use of low energy ions as found in inductively-coupled-plasma (ICP) in conjunction with post-etch anneal can alleviate damage problems significantly. Control of the ICP step is another important fact for getting well recessed gates.

CF_4 plasma has been involved in the processing of AlGaN/GaN HEMTs, mainly for dry etching the SiN_x dielectric layer. Recently, a simple approach based on a surface selective CF_4 plasma treatment of the AlGaN/GaN HEMT gate area was introduced to reduce the gate leakage current [9] and current collapse [10]. It was recently discovered that CF_4 plasma treatment plays an important role in the electrical behavior of AlGaN/GaN HEMTs. The CF_4 plasma treatment has been demonstrated to shift the threshold voltage of AlGaN/GaN HEMTs toward positive bias, thus enabling enhancement-mode operation [7,11–13]. Additionally, it

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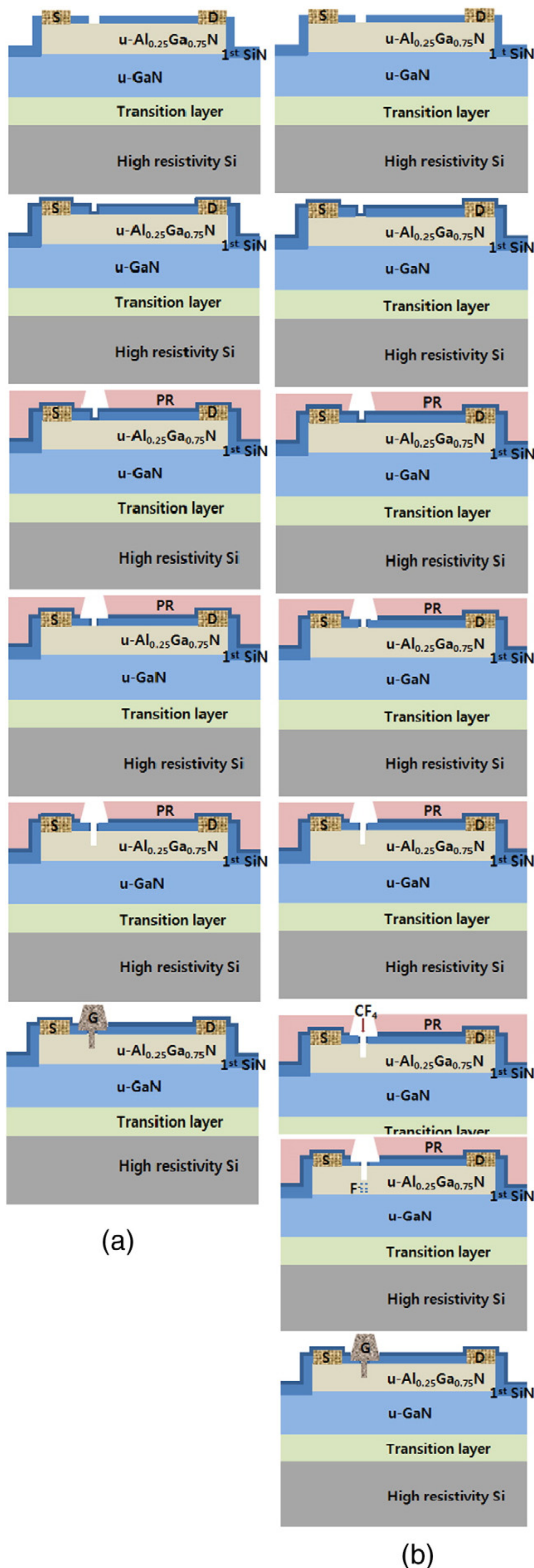

Fig. 1. Cross-sectional view of the 0.5 μm AlGaN/GaN. HEMTs: (a) sample A and (b) sample B.

was reported that exposure of AlGaN/GaN HEMTs to CF_4 plasma prior to gate metallization can significantly suppress gate leakage [14].

In this study, we demonstrate the fabrication of enhancement-mode AlGaN/GaN HEMTs using double plasma treatment process. The AlGaN/GaN HEMTs with different recess etching treatments, including BCl_3/Cl_2 plasma and low damage CF_4 plasma etching, were fabricated and compared with BCl_3/Cl_2 plasma recessed devices. To achieve the AlGaN/GaN HEMTs from depletion-mode (D-mode) to E-mode, the dielectric etch and gate recess processes have been adopted include two separate plasma treatment steps. It will be shown that E-mode AlGaN/GaN HEMTs fabricated using double plasma treatment process exhibit good DC and microwave characteristics.

2. Experiment

The AlGaN/GaN HEMT epitaxial structure was grown by metal–organic chemical vapor deposition on a 4-in (111) silicon substrate and consists of the following layers: a transition layer, a 2-μm-thick undoped GaN buffer layer, and a 250 Å $Al_{0.25}Ga_{0.75}N$ Schottky contact layer. Finally, a 20 Å thick undoped GaN cap layer was grown to protect the active layer.

The process flow is illustrated in Fig. 1. At first, device mesa was defined by conventional photolithography. The AlGaN/GaN was etched down to the GaN buffer layer using BCl_3/Cl_2 plasma dry etching in an ICP system.

The ohmic contact patterns were defined using a lift-off technique. A Ti/Al/Ni/Au metal system was used for the source and drain since it is widely used as an ohmic contact to GaN materials. Prior to the contact deposition, the wafers were cleaned by dipping into a HCl:H_2O solution; they were then rinsed in deionized water and blown dry with nitrogen. They were loaded into an e-beam evaporation system, and the vacuum system was pumped to 6.7×10^{-5} Pa before contact deposition. Then, the Ti/Al/Ni/Au ohmic contact structure was deposited on the undoped GaN cap layer. The Ti/Al/Ni/Au layer thicknesses were 300, 1000, 300 and 1000 Å. These ohmic contacts were heat-treated by rapid thermal annealing in a nitrogen atmosphere. The ohmic contact alloying was performed 850 °C for 30 s. The contacts were then examined electrically using transmission line model measurements. The specific contact resistivity ρ_c was $5.1 \times 10^{-6}\ \Omega \cdot cm^2$. A 700 Å silicon nitride layer was deposited by plasma enhanced chemical vapor deposition at 260 °C to protect the device and to support the gate. The gate footprint patterning was done by conventional photolithography. After development of the resist, the SiN_x was etched by reactive ion etching system. The SiN_x layer was etched using CF_4 plasma alone to create a 0.5 μm gate footprint. And then, a 150 Å SiN_x was deposited on all of the samples to obtain the reduction of gate length. The top of the gate was defined by conventional photolithography. After development of the resist, the gate recess was done by ICP dry etching using a BCl_3/Cl_2 gas mixture. The gate recessing of sample A was performed using an ICP etching process, and that of sample B was carried out in two steps including a reactive-ion etching (RIE) process. The gate recess is stopped when a predetermined source–drain current is reached. After the gate recess and CF_4 plasma treatment, Ni/Au layers (3600 Å) were deposited and lifted-off. Fig. 2 shows a photograph of fabricated AlGaN/GaN HEMT unit gate with 150 μm wide and two-finger.

3. Results and discussion

AlGaN/GaN HEMTs with source-to-drain spacings of 3 μm, source-to-gate spacings of 0.8 μm, gate-to-drain spacings of 1.7 μm, unit gate widths of 150 μm, two gate fingers, and gate lengths of 0.5 μm were fabricated using the conventional photolithography on the AlGaN/GaN HEMT structure. This asymmetric source and drain structure

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