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Uniaxial stress effect and hole mobility in high-Ge content strained SiGe (110) P-channel metal oxide semiconductor field effect transistors

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ABSTRACT

The hole mobility in a high Ge-content (110) SiGe inversion layer is measured and simulated by a split capacitance–voltage method and a quantized $\vec{k} \cdot \vec{p}$ method, respectively. The calibrated model reproduces our experimental channel mobility measurements for the biaxial compressive strain SiGe on (110) substrate. We also explore the impact of external mechanical uniaxial stress on the SiGe (110) p-channel metal oxide semiconductor field effect transistor (PMOSFET). We obtained the corresponding piezoresistance coefficients of the SiGe (110) PMOSFET with external mechanical uniaxial stress parallel and perpendicular to the channel direction. Our study shows the effectiveness in combining external mechanical uniaxial stress and intrinsic biaxial compressive strain for the SiGe (110) PMOSFET.

1. Introduction

High Ge-content SiGe channels under strain for increased mobility have attracted significant attention for potential use in next-generation Complementary Metal Oxide Semiconductor [1,2] technology. Due to the enhanced mobility of strain engineering, the high Ge content channel with strain is a worthy technology. Ultra-thin epitaxially-grown SiGe (epi-SiGe) on Si with compressive strain has the advantages of high mobility, low cost, and compatibility with current Si manufacturing processes. Ge concentrations as high as 80% mole fraction in the SiGe channel have been reported on Si (100) and (111) with 200% and 110% hole mobility enhancements, respectively [3,4]. However, the substrate orientation and carrier transportation direction should be optimized for mobility enhancement. For a p-channel Metal–Oxide–Semiconductor Field Effect Transistor (PMOSFET) performance enhancement, the <110>/(110) has approximately 150% hole mobility enhancement compared to the <110>/(100) Si channel [5]. The lower Ge channel, $Si_{0.7}Ge_{0.3}$ and $Si_{0.4}Ge_{0.6}$, on Si (110) has recently been reported with peak mobilities of 210 and 340 cm^2/Vs, respectively [6,7]. The high Ge mole fraction (greater than 80%) in SiGe easily self-assembles into Ge islands for strain relaxation during epitaxy on a Si (110) surface. This self-assembly of Ge islands occurs due to the (110) surface having the highest surface energy and being unstable to faceting; because of the twofold symmetry of the surface for atomic processes [8]. The critical thickness should be thinner on (110) than (100) for epitaxial growths. Furthermore, Si (110) has {111} cleavage planes perpendicular to the surface, which may assist carrier transportation (e.g. band offsets) for hetero-junction device applications. The channel mobility can be enhanced by optimizing the channel direction and the surface orientation of the substrate. Due to various stresses and different surface orientations, the valence band is reshaped, resulting in a change in the effective mass and matrix elements of phonon and surface roughness scattering. For (001) surface orientation, hole mobility modeling of uniaxially strained Si bulk PMOSFET structures has been studied intensively based on the quasi two-dimensional (2D) hole gas subband structure [11,12]. We extended the above theoretical work to reproduce measured mobility results for our SiGe PMOSFET. In this paper, external mechanical uniaxial and intrinsic biaxial strain owing to lattice mismatch between the epitaxially-grown layer and substrate additive mobility enhancements and their physical characteristics are used to experimentally apply mechanical uniaxial stress to the (110) SiGe channel materials. We herein focus on the development of strained SiGe on Si (110) substrates for use as PMOSFETs. Experimental and theoretical studies on the hole mobility in the SiGe (110) PMOSFET under external mechanical uniaxial stress are discussed in detail. In Section 2, we discuss the fabrication and mechanical bending apparatus for use in the SiGe (110) PMOSFET. In Section 3, split capacitance–voltage (C–V) measurements and theoretical treatment of the hole mobility of the high-Ge content SiGe are presented. Experimental and calculated results are then provided in Section 4. The paper is summarized in Section 5.

2. Device preparation and the mechanical uniaxial stress condition

Starting from (100), (110) and (111) Si substrates with a resistivity of 15–25 Ω-cm, a thin SiGe channel with a thin Si cap as the passivation layer was selectively grown at 525 °C using ultrahigh-vacuum chemical vapor deposition (UHV-CVD) and SiH_4 and GeH_4 precursors. He carrier

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gas was used on the active region after isolation and the well implant process. The low temperature growth in the UHV-CVD at 525 °C can increase the critical thickness due to kinetically limited growth. A nominally 4 nm Si cap was grown on the top of the epi-SiGe to passivate and smoothen the surface. The sacrificial Si cap was reduced to approximately 1 nm and the thickness of the SiGe layer was about 5 nm after processing. Note that the expected mole fraction of approximately 80% Ge for the SiGe film at the final stage was confirmed using H-scan X-ray diffraction. It should also be noted that the SiGe layer has about 2.5% biaxial compressive strain. The gate stack consisted of an approximately 300 nm tetra-ethyl-oxy-silane (TEOS) gate dielectric and a poly Si gate electrode. The source/drain (S/D) with BF_2 implantation was activated by rapid excimer laser thermal annealing (RTA) at 600 °C for 100 s. The one-mask device fabrication process flow and the device structure are shown in Fig. 1. Si substrates with (001), (110), and (111) surface orientations were used for our devices. The epi-SiGe was grown with an Si capping layer using UHV-CVD. In the third step, a TEOS gate dielectric layer and a poly Si gate electrode were deposited. Optical lithography and photoresist trimming were then employed for gate patterning. After the gate etch process was complete, the S/D region was formed using BF_2 implantation. This was followed by rapid excimer laser thermal annealing (RTA) at 600 °C for 100 s. After all processes were complete, the sacrificial Si cap was reduced to approximately 1 nm. The one-mask process to fabricate our SiGe PMOSFET was then completed.

In a wafer bending apparatus [9], different stresses were applied on long channel devices, and piezoresistance coefficients were obtained from the slope of drive current gain versus applied stress. Our bending setup was used to apply uniaxial stress up to 260 MPa. The bending setup was calibrated with a load cell under the mounting platform and a strain gauge mounted on to the surface of the wafer. Two wafer bending conditions were applied: a uniaxial compressive stress parallel to the channel direction for a longitudinal piezoresistance coefficient, and a uniaxial tensile stress perpendicular to the channel direction for a transverse piezoresistance coefficient.

3. Hole mobility measurement and calculation

3.1. Split C–V method

To accurately extract the carrier mobility, the split C–V method [10] is used to characterize the inversion charge density and effective electric field for our SiGe channel PMOSFET devices. The effective electric field (E_{eff}) is defined by

$$E_{eff} = \frac{q}{\varepsilon}\left(N_{dep} + \frac{1}{3}N_{inv}\right), \tag{1}$$

where q is the elementary charge, ε is the permittivity, N_{dep} is the surface concentration of the depletion charge, and N_{inv} is the surface inversion carrier concentration. The effective mobility in the inversion layer, μ_{eff}, was determined from the drain conductance g_d in the linear region as

$$\mu_{eff} = \frac{L}{W}\frac{g_d\left(V_g\right)}{qN_{inv}\left(V_g\right)} \tag{2}$$

where g_d was measured at the drain voltage of 50 mV. The surface carrier concentration, N_{inv}, was determined directly through the measurement of gate-channel capacitance $C_{gc}(V_g)$;

$$qN_{inv}\left(V_g\right) = \int_{-\infty}^{Vg} C_{gc}\left(V_g\right)dV_g. \tag{3}$$

The measurement frequency was set as low as possible in order to avoid the influence of the resistive component of the channel. The carrier mobility was experimentally extracted at different effective electric fields. The simulated carrier mobility was calculated with the same inversion charge density for comparison.

3.2. Kubo–Greenwood formula

The simulations are based on the self-consistent solution of the 6 × 6, Schrödinger Equation (SE) and Poisson Equation (PE) [11,12]. This simulation method captures the influence of the size quantization, strain, surface/channel orientations, and the SiGe alloys on a solid physical basis. Each device is partitioned into many vertical slices along the channel direction [11]. The 1D SE is solved for each slice. The biaxial compressive strain tensor is determined based on the Ge content of the SiGe in the channel layer and the substrate. The Pikus–Bir strain Hamiltonian is calculated using the resultant strain tensor and added to the 6 × 6 $\vec{k}\cdot\vec{p}$ Hamiltonian. The diagonal Hamiltonian resulting from these valence band offsets is also added to the total Hamiltonian. Spin-orbit coupling is considered by the additional spin-orbit coupling Hamiltonian. Size quantization effects and the electrostatic potential are considered by solving the 1D 6 × 6 $\vec{k}\cdot\vec{p}$ envelope function SE which results from the total Hamiltonian. The solution of the SE provides the valence subband structure and allows the calculation of the scattering overlap factors. A rotation of the 6 × 6 $\vec{k}\cdot\vec{p}$ Hamiltonian and the strain Hamiltonian is necessary in order to handle different surface orientations [11]. The hole density resulting from the subband structure and the distribution function is considered in the 2D PE in order to obtain a self-consistent solution. In this work, subband structure calculations are calculated using nextnano3. We have calculated the hole mobility for the SiGe (110) PMOSFET using the Momentum Relaxation Time (MRT) approximation according to the Kubo–Greenwood formulation [11,12]. The scattering mechanisms included in our calculations are the acoustic and optical phonons, the surface roughness scattering, alloy scattering, and Coulomb scattering. The difficulties related to the calculation of the MRT in inversion layers have been discussed in detail in [11,12], together with the approximations that are typically used in order to obtain explicit, relatively simple expressions. The formulation of the relaxation time for the different scattering mechanisms used in this paper follows the treatment in [11,12]. Note that we follow a fully numerical procedure as proposed by [13] for the calculation of the Coulomb scattering (CS) potential induced by a point charge arbitrarily located in the semiconductor, in the oxide, in the semiconductor/oxide interface or in the poly silicon gate electrode. This procedure also includes the corresponding results for the remote Coulomb scattering (RCS) such as interface trap (D_{it}) scattering. When the channel contains SiGe-alloy material, the alloy scattering also needs to be taken into account. In the Harrison and Hauser model for the bulk case [14], a wide range of values between 0.2 and 1.0 eV has been reported in the

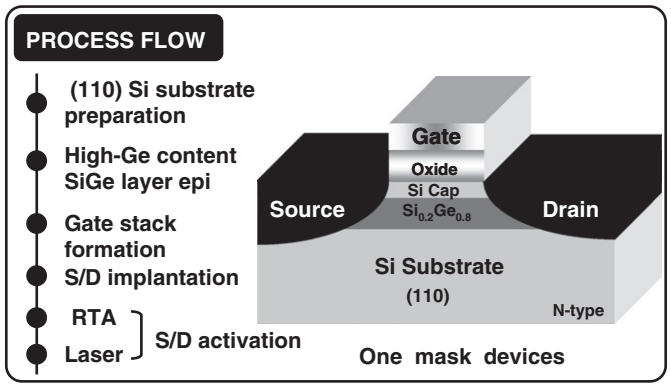

Fig. 1. The device fabrication process flow and device structure. After all processes are complete, the sacrificial Si cap was reduced to approximately 1 nm.