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Pathways toward higher performance CdS/CdTe devices: Te exposure of CdTe surface before ZnTe:Cu/Ti contacting

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ABSTRACT

Many studies of thin-film CdS/CdTe photovoltaic devices have suggested that performance may be improved by reducing recombination due to Te-vacancy (V_{Te}), Te antisite (Te_{Cd}), or Te-interstitial (Te_i) defects. Although formation of these intrinsic defects is likely influenced by CdTe deposition parameters, it may be also coupled to the formation of beneficial cadmium vacancy (V_{Cd}) defects. In this study, we expose the CdTe surface to Te vapor prior to ZnTe:Cu/Ti contact-interface formation with the goal of reducing V_{Te} without significantly reducing V_{Cd}. Initial results show that when this modified contact is used on a $CdCl_2$-treated CdS/CdTe device, poorer device performance results. This suggests two things: First, the amount of free-Te available during contact formation (either from chemical etching or Cu_xTe or ZnTe deposition) may be a more important parameter to device performance than previously appreciated. Second, if processes have been used to reduce the effect of V_{Te} (e.g., oxygen and chlorine additions), adding even a small amount of Te may produce detrimental defects.

1. Introduction

Previous studies indicate that performance limitation in present polycrystalline CdS/CdTe devices may originate from high recombination in the quasi-neutral region [1]. Although some control of CdTe recombination has been achieved historically through the careful incorporation of the extrinsic impurities, oxygen, chlorine, and copper [1,2], many technologists believe that a more promising avenue to improve CdTe photovoltaic device performance is to understand the intrinsic CdTe defects that may form during high-rate (i.e., non-equilibrium) CdTe deposition processes. This is supported by theoretical studies that suggest that much of the improvement associated with oxygen, chlorine, and copper is due to their interaction with cadmium and tellurium vacancies (V_{Cd} and V_{Te}, respectively) [3,4].

For CdS/CdTe superstrate devices, we believe most junction-formation processes can be viewed through the following sequence of defect-formation processes: CdTe is deposited from a nominally stoichiometric source where, depending on source manufacture, pre-conditioning, and deposition conditions, the resulting CdTe film can entrain a Te or Cd deficiency (e.g., ~0.01 at.% at thermodynamic equilibrium) [5]. This can lead to the formation of various intrinsic defects, including Te and Cd vacancies and/or interstitials. Of these, the Te vacancies, antisites, and interstitials are more problematic because all are predicted to be mid-gap defects, and thus could limit minority-carrier lifetime [3]. Both oxygen (either intentional or unintentionally added during CdTe deposition) and Cl (added during the post-deposition $CdCl_2$ treatment) may help limit the detrimental effect of V_{Te} through substitution on the V_{Te} site and subsequent formation of defect pairs with cadmium vacancies (i.e., $V_{Cd}+O_{Te}$ and $V_{Cd}+Cl_{Te}$) [6]. These defect pairs may not only reduce the concentration of V_{Te} but also provide shallower acceptors than the singly ionized V_{Cd} defects they replace, thus making the CdTe layer more p-type at typical operating temperatures [3]. Following the $CdCl_2$ treatment, Cu diffusion from a Cu-containing contact further increases the net-acceptor concentration (N_A–N_D) by displacing Cd to form Cu_{Cd} acceptor defects. Optimal concentration of these defects will increase N_A–N_D and reduce the junction space-charge width (W_D). However, further Cu diffusion above the optimal concentration may reduce N_A–N_D through the formation of Cu interstitial donor (Cu_i) defects [4]. Optimum device performance is attained when W_D (controlled by the formation of $V_{Cd}+O_{Te}$, $V_{Cd}+Cl_{Te}$, and Cu_{Cd}) is narrow enough to produce a drift field in the CdTe absorber that is sufficiently strong to overcome the relatively poor lifetime of the minority carriers (controlled by the presence or formation of V_{Te}, Te_{Cd}, Te_i, and Cu_i), but still wide enough to limit the effects of voltage-dependent collection (i.e., photocarriers should be generated primarily within the depletion region when the device is biased near the maximum-power point) [1]. Studies additionally suggest that optimum Cu diffusion conditions can increase minority-carrier lifetime and thus increase device performance [2].

In contrast to this relatively complicated description, we believe that an alternative pathway to produce CdTe layers with superior

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material quality may be to control the formation of intrinsic CdTe defects by modifying deposition and/or post-deposition processes. In this study, we report on one post-deposition process where the CdTe back surface is exposed to Te vapor prior to the application of a ZnTe:Cu/Ti contact. These initial results suggest that establishing a high-rate CdTe deposition process that can limit both the formation of V_{Te} (i.e., insufficient Te) and Te_{Cd} or Te_i (i.e., excess Te) may be an important pathway to improved device performance.

2. Experimental details

The superstrate devices used for this study had the structure of glass/SnO_2:F/SnO_2/CdS:O/CdTe/ZnTe:Cu/Ti. The glass was 1-mm aluminosilicate, while the TCO and CdS:O layers were deposited by chemical vapor deposition (500 nm) and chemical bath deposition (80 nm), respectively. The CdTe layers were 4-μm thick, were deposited by close-space sublimation at 600 °C, and were treated in $CdCl_2$ vapor at 400 °C for 5 min. The ZnTe:Cu/Ti contact was produced by placing the $CdCl_2$-treated samples into a multisource vacuum chamber, preheating for 120 min to 340 °C, and then removing ~100 nm of CdTe using Ar ion-beam milling. ZnTe:Cu layers (2 wt.% Cu) were deposited by radio-frequency (RF) sputtering to a thickness of 400 nm followed by depositing 500 nm of Ti using direct-current (DC) magnetron sputtering. For Te-exposed samples, the $CdCl_2$-treated back surface was exposed to a Te vapor during preheat to 340 °C (i.e., before the ion-beam milling step) in the same chamber as used for contact deposition. The amount of Te incorporated into the CdTe film during this process has not been established. However, because its influence is observed following ion-beam removal of ~100 nm of material from the surface (mostly CdTe), we believe the Te is incorporated into the CdTe film, rather than residing only as a surface layer.

Processing to form 0.25-cm^2 cells included photolithography followed by two-step chemical etching, first using TFT Ti Etchant (Transene Co. Inc., Rowley, MA) to remove the Ti, followed by an aqueous solution of 39% $FeCl_3$ to remove the ZnTe:Cu and CdTe. A perimeter contact onto the SnO_2 layer was formed with soldered indium. Electrical analysis of the resulting devices included light/dark current voltage (LIV/DIV) measurements using an XT-10 solar simulator adjusted to approximate Global AM1.5 current from a CdS/CdTe reference cell, and capacitance-voltage (CV) measurements that were performed in the dark using an HP 4294A impedance analyzer at a frequency of 100 kHz and a voltage-bias range of +0.2 to −1.0 V. Optical measurements included room-temperature spectroscopic photoluminescence (RTPL), low-temperature (4 K) spectroscopic photoluminescence (LTPL), and room-temperature time-resolved photoluminescence (TRPL) measurements. All PL measurements were taken from the glass side of the superstrate devices and additional experimental details are provided elsewhere [2]. Compositional analysis of Cu diffusion was performed by secondary ion mass spectrometry (SIMS) from the contacted side of the devices, using a Cameca IMS-5F instrument with oxygen as the primary ion source and tuned for a mass resolution (M/ΔM) of ~4000 to allow for separation of $^{63}Cu^+$ from $^{126}Te^{2+}$ species.

3. Results

Fig. 1 shows a sequence of LIV curves detailing the change in performance of CdS/CdTe devices before and after Te exposure of the back contact. Before Te exposure, devices demonstrate an efficiency of ~14% (see device 14480 in Fig. 1), typical for NREL CdS/CdTe devices made using the processes described above. Immediately following Te exposure, the performance drops to ~1% (see device 14501 in Fig. 1). The figure also shows that the ~14% baseline is not re-established until ~4–6 additional devices are contacted in the same vacuum chamber, but without Te exposure. Re-establishing the performance baseline is promoted further by cleaning the chamber using a thermal treatment (see device 14505 in Fig. 1). This trend has been confirmed in several different run sequences. At this time, efforts to link this functionality to other process steps (i.e., CdS, CdTe, or $CdCl_2$) have been unsuccessful. The LIV performance trend shown in Fig. 1 is different from that observed previously in CdS/CdTe devices produced with an NREL-ZnTe:Cu/Ti or an NREL-paste contact. Although previous studies indicate that open-circuit voltage (V_{oc}), fill factor, and short-circuit current (J_{sc}) are reduced when insufficient Cu diffuses from the contact into the CdTe (all manifestations of low N_A–N_D) [1], overall performance this low, and related only to the pre-contacting process, has not been observed.

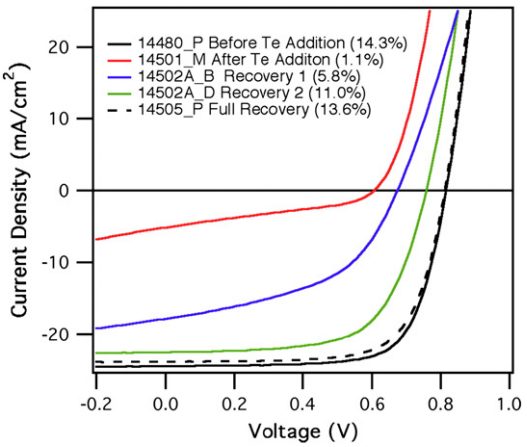

Fig. 1. Light current–voltage (LIV) characteristics of CdS/CdTe devices produced before and after Te exposure prior to the ZnTe:Cu/Ti contacting process.

CV analysis (Fig. 2) reveals that Te exposure causes the space charge to become wide and relatively insensitive to device bias. As the chamber is used for subsequent runs, the space charge re-establishes a profile consistent with high-performance devices [1]. Numerical simulations have shown that this functionality is consistent with the appearance of deep defects in the CdTe layer following Te exposure [7]. Fig. 3 shows TRPL measurements of devices produced at various times following Te exposure of the CdTe back surface (Set A, Table 1). The data show the bi-exponential trend observed previously in CdS/CdTe devices, from which both a fast (τ_1) and slow (τ_2) recombination rate can be calculated [2]. Although τ_1 and τ_2 each become significantly shorter following Te exposure, both of these parameters recover as the vacuum system is used for subsequent depositions. Table 1 lists τ_1 and τ_2 values for various sets of samples used in this study. It is worth noting that, for all

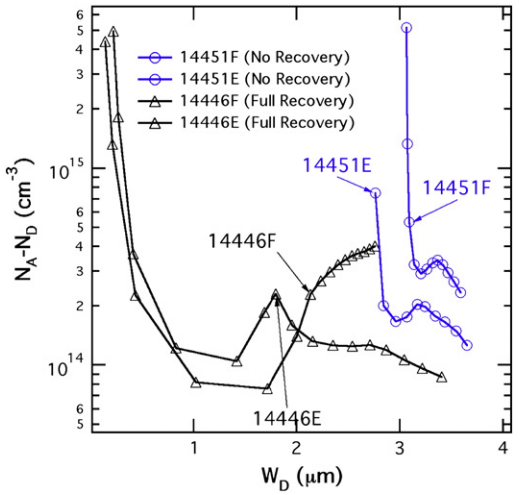

Fig. 2. Dark CV data showing changes in net-acceptor doping profile as a function of recovery state indicated in Table 1. Arrow indicates location of zero-bias depletion width.