



Influence of S/Se ratio on series resistance and on dominant recombination pathway in $\text{Cu}_2\text{ZnSn}(\text{SSe})_4$ thin film solar cells

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ABSTRACT

$\text{Cu}_2\text{ZnSn}(\text{SSe})_4$ and CuZnSnSe_4 thin film solar cells are analyzed via temperature dependent current–voltage analysis and quantum efficiency measurements in order to study the dominant recombination pathway and the temperature dependence of the series resistance. Here we show that in contrast to mixed S/Se devices, solar cells where the absorber consists of selenide only do not exhibit interface recombination and the series resistance is small in the complete investigated temperature range. The recombination path difference supports a band alignment model with a cliff for S and a spike for Se. The measurements are supplemented with secondary ion mass spectrometry measurements in order to gain insights into the physical origin of the different device characteristics. The results suggest that the high series resistance originates from a $\text{ZnS}(\text{e})$ secondary phase which is situated at the $\text{Cu}_2\text{ZnSn}(\text{SSe})_4/\text{CdS}$ heterojunction.

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1. Introduction

$\text{Cu}_2\text{ZnSn}(\text{SSe})_4$ (CZTSSe) thin film solar cells are promising candidates for high efficiency and cost effective thin film solar cells since most elements are highly abundant in the earth crust and the fundamental optoelectronic properties are suitable for photovoltaic applications. The solar cell efficiencies have been improved substantially in the last two years by a number of groups. The best sulfur (CZTS) device achieved a power conversion efficiency of 8.4% [1], the mixed CZTSSe a record efficiency of 10.1% [2] and the pure Se devices (CZTSe) reached a maximum efficiency of 9.1% [3]. In order to further improve the CZTSSe devices it is indispensable to investigate which properties of the solar cells are currently limiting the performance. A detailed comparison of the properties of CZTSSe with different S/Se ratios has been published by Mitzi et al. [4]. They concluded that one major problem, which limits the open-circuit voltage is interface recombination. In this case the interface bandgap is smaller than the bulk bandgap which can arise due to an unoptimized band-alignment (cliff like conduction band offset), Fermi-level pinning or a non-optimized absorber window doping [5]. Experimental measurements of the band-alignment between the CZTSSe and the CdS buffer layer are contradictory. Haight et al. [6] studied CZTSSe absorbers and concluded that the conduction band offset is type I, i.e. a spike independent of the S/Se ratio. In another study Bäer et al. [7] studied CZTS absorber layers and concluded that the band offset would be of type II, i.e. a cliff.

In addition to the limitations imposed by interface recombination almost all the devices described in literature exhibit a high series

resistance and a crossover between the dark and the illuminated current–voltage curves [4]. The series resistance increases almost exponentially towards lower temperature. This behavior has been assigned to a blocking backcontact barrier between the Mo and the CZTSSe [8]. A large barrier at the $\text{Mo}/\text{MoS}(\text{e})_2/\text{CZTSSe}$ interface suppresses the injecting of the majority carriers. Only recently Bag et al. [9] demonstrated that the series resistance is much lower in almost pure Se devices [$S/(S + \text{Se}) = 0.03$]. However the solar cell was still limited by interface recombination.

Both observations point towards non-optimized buffer layers and backcontacts for CZTSSe. Finally the investigated CZTSSe absorber layers [4] have a relatively low minority carrier lifetime as deduced from time resolved photoluminescence. In this paper we address the problem of interface recombination and high series resistance. We will show that the restrictions observed by Mitzi et al. [4] are not universal and depend on the S/Se ratio of the absorber.

2. Experimental details

The CZTSe absorbers have been produced via a precursor/annealing routine where first a precursor layer has been prepared via coevaporation of Cu, Sn, Zn and Se in a molecular beam epitaxy apparatus. The deposition has been carried out on molybdenum coated soda lime glass at a temperature of 320 °C. In a second step the absorber layers have been annealed in a tube furnace in an H_2/N_2 environment (1 mbar total pressure). The samples are placed in a graphite box together with additional Se and SnSe or Sn. Details of the annealing can be found elsewhere [10]. The Sn source is necessary to ensure that volatile SnSe is not lost from the absorber layer during the heat treatment. In the case of mixed S/Se absorbers the procedure is very similar to the Se case except during

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the final heat treatment additional S and SnS or Sn have been included in the box. Part of the Se is exchanged with S and a mixed SSe absorber layer is formed. In both cases Cu-poor ($\text{Cu}/(\text{Zn} + \text{Sn}) < 1$) and Zn-rich ($\text{Zn}/\text{Sn} > 1$) absorbers have been produced. The Se-absorber characterized via 20 keV energy dispersive X-ray analysis (EDX) measurements has a composition of $\text{Cu}/(\text{Zn} + \text{Sn}) = 0.8$ and $\text{Zn}/\text{Sn} = 1.3$ whereas the SSe-absorber has a composition of $\text{Cu}/(\text{Zn} + \text{Sn}) = 0.9$ and $\text{Zn}/\text{Sn} = 1.1$.

Solar cells have been fabricated as follows. After absorber processing the samples are etched in 5 wt.% KCN for 30 s in order to remove any remaining Cu_xSe . In the next step a CdS buffer layer is deposited via chemical bath deposition followed by magnetron sputtering of i-ZnO and Al-doped ZnO which acts as the n-type window layer. The cells are finalized via e-beam evaporation of Ni–Al grids for front contacting.

The solar cells are characterized with a home-built current–voltage setup (IV) equipped with a halogen lamp as light source. The system is calibrated to $100 \text{ mW}/\text{cm}^2$. Temperature dependent IV-analysis (IVT) has been performed between room temperature and 120 K. The temperature of the absorber layer has been measured during the cooling/heating cycles with a Si-diode connected on top of a dummy cell in order to get an accurate temperature measure. The light source is identical to the light source in the IV-setup. Contacting has been carried out with epoxy glue on the front and the back contacts. All solar cell parameters have been extracted with the method introduced by Sites et al. [11]. The solar cells have been further characterized with a home-built Quantum Efficiency (QE) apparatus in order to extract the bandgap of the solar cell.

Depth profiles have been carried out via secondary ion mass spectrometry (SIMS) where Cs^+ ions are used for sputtering and positively charged Cs-metal clusters are detected.

In the following the discussion is limited to a detailed comparison of two devices where the one is a pure Se device and the other one a

SSe-device. The conclusions are not limited to these two samples but the trends and the important observations have been checked for a number of S and SSe-devices.

3. Results and discussion

Fig. 1 shows a comparison of two kesterite thin film solar cells with efficiencies higher than 6%. In Fig. 1(a) the absorber has been produced without sulfur (denoted Se-device) whereas Fig. 1(b) shows a device where the absorber layer contains sulfur and selenium (denoted SSe-device). The solar cell parameters are indicated below the IV-curves. Already at first sight there are quite some differences between the devices. First the sulfur free solar cell has a much lower open circuit voltage than the mixed device and a much higher short circuit density. This is a direct consequence of the different bandgaps of the absorber layers. CZTSe has a bandgap of roughly 1 eV whereas a pure CZTS absorber exhibits a bandgap of 1.5 eV [12]. A mixed absorber layer has a bandgap between the two extrema depending on the S/Se ratio. In our case a bandgap of 0.93 eV has been extracted for the Se-device and 1.23 eV for the SSe-device. The bandgap is extracted from a linear extrapolation of the low energy slope of the QE measurements as shown in Fig. 1(c), (d). Moreover, the SSe device has a much higher series resistance R_s than the Se-device ($2.7 \Omega \text{ cm}^2$ compared to $0.6 \Omega \text{ cm}^2$). The high series resistance of the SSe-device can be considered as typical compared to the devices described in literature. The series resistance of the Se-device is much lower and a value below $1 \Omega \text{ cm}^2$ can be considered as unproblematic for the device operation. It has to be emphasized that a low value of R_s has also been reported for a Se-device by Repins et al. [3]. The losses in fill factor (FF) arise from the parasitic resistances and due to the rather high J_0 of the devices.

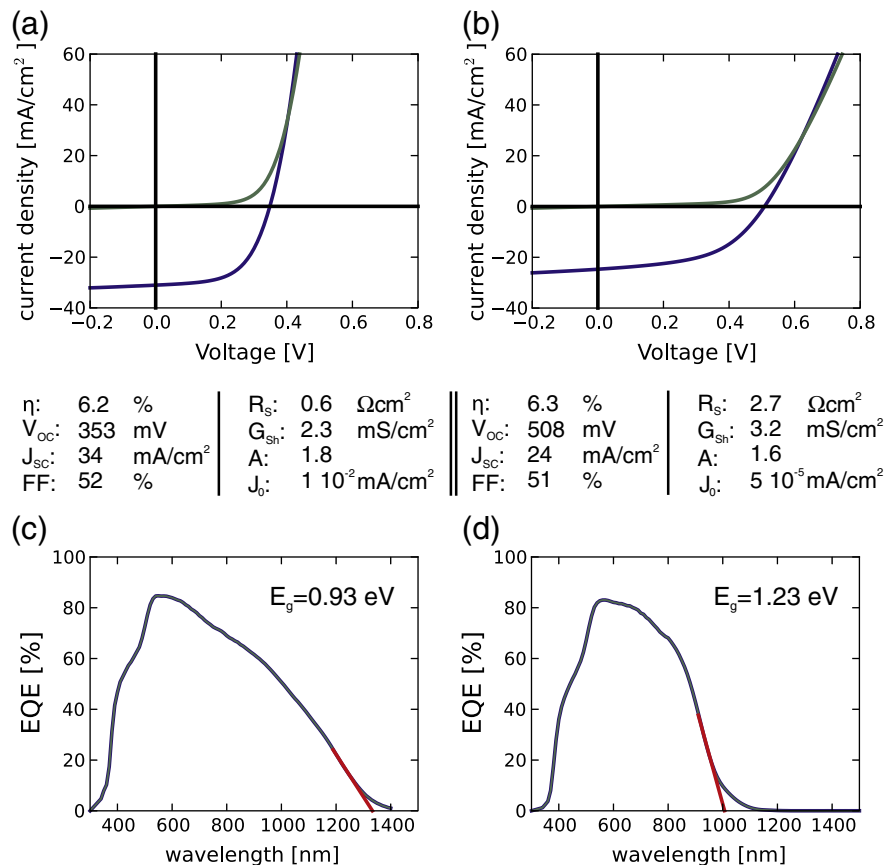


Fig. 1. Current–voltage characteristics and parameters of (a) the CZTSe device and (b) CZTSSe device. (c), (d) Quantum efficiency measurements of the devices shown in (a) and (b). Bandgaps E_g are deduced via linear extrapolation of the low energy slope of the QE as shown in the corresponding figures.

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