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Ultrathin HfON/SiO_2 dual tunneling layer for improving the electrical properties of metal–oxide–nitride–oxide–silicon memory

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ABSTRACT

A high-k gate stack structure with ultrathin HfON/SiO_2 as dual tunneling layer (DTL), AlN as charge storage layer (CSL) and HfAlO as blocking layer (BL) is proposed to make a charge-trapping-type metal–oxide–nitride–oxide–silicon non-volatile memory device by employing in-situ sputtering method. The validity of the structure is examined and confirmed by transmission electron microscopy. The memory window, program/erase, endurance and retention properties are investigated and compared with similar gate stack structure with Si_3N_4/SiO_2 as DTL, HfO_2 as CSL and Al_2O_3 as BL. Results show that a large memory window of 3.55 V at a program/erase (P/E) voltage of +8 V/−15 V, high P/E speed, and good endurance and retention characteristic can be achieved using the Au/ HfAlO/AlN/(HfON/SiO_2)/Si gate stack structure. The main mechanisms lie in the enhanced electron injection through the ultrathin high-k HfON/SiO_2 DTL with suitable band offset, high trapping efficiency of the high-k AlN material, and effective blocking role of the high-k HfAlO BL.

1. Introduction

The challenges for non-volatile memory devices are to achieve high program/erase (P/E) speed at low operating voltage, large memory window and good 10-year data retention simultaneously [1]. Because of the advantages in scaling, simple fabrication process and robustness against defect-related leakage, metal–oxide–nitride–oxide–silicon (MONOS) memory devices become attractive candidates [2]. Extensive researches have been performed in recent years, involving the use of high-k HfO_2 [2,3] or AlN [1,4,5] as charge storage layer (CSL), the use of Si_3N_4/SiO_2 [2] or ZrO_2/SiO_2 [6] as dual tunneling layer (DTL) to enhance the tunneling current, the use of Al_2O_3 instead of SiO_2 as the blocking layer (BL) [7,8] and the use of high-work-function metal gate [9,10] for suppressing electron injection from gate electrode. Bandgap-engineered MONOS with dual tunneling layer can offer a compromise among the improvements of memory window, program/erase speeds and retention, due to the increased conduction-band offset (ΔE_C) and valence-band offset (ΔE_V) of the high-k layer relative to SiO_2. However, little work concentrated on combining the advantages of high-k BL and CSL with the band-engineered dual tunneling layer of high-k/SiO_2. In this work, we propose a high-k gate stack structure — Au/HfAlO/AlN/(HfON/SiO_2)/Si for MONOS memory applications which combines an ultrathin DTL of HfON/SiO_2 with the high-k HfAlO BL [11,12] and AlN CSL to comprehensively improve the performances of the devices. Here, the use of HfAlO instead of Al_2O_3 as BL is because a higher dielectric constant can be obtained due to combination of HfO_2 with Al_2O_3. As a result, a high coupling ratio under the same physical thickness can be generated due to the smaller equivalent oxide thickness (EOT), and also, the large barrier height and good thermal stability of HfAlO can be obtained by controlling the amount of Al_2O_3 in the film at reasonable value. The electrical characteristics of the proposed device are evaluated through comparison with a similar high-k gate stack structure of Au/Al_2O_3/HfO_2/(Si_3N_4/SiO_2)/Si as reported in [2], because many researchers used the Si_3N_4/SiO_2, HfO_2 and Al_2O_3 as DTL [13–15], CSL [2,3] and BL [16,17] respectively, demonstrating good performances and their combination could be expected as one of the promising bandgap-engineered candidates to improve the program/erase speed, memory window and charge retention characteristics. Experimental results indicate that the large memory window, high program/erase speed at low operating voltage and good retention property can be obtained by using the proposed high-k gate stack structure.

2. Experiments

To improve the P/E characteristics of MONOS flash memory device, a high-k stack gate dielectric structure of Au/HfAlO/AlN/(HfON/SiO_2)/Si is proposed, with ultrathin HfON/SiO_2 as double tunneling layer, AlN as charge-storage layer and HfAlO as blocking layer, as shown in Table 1. These high-k dielectrics were consecutively deposited in-situ by reactive sputtering (or co-sputtering) method using Denton Vacuum Discovery Deposition System at room temperature. A 2-nm thick SiO_2 was thermally grown in dry O_2 at 900 °C on

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Table 1
High-k gate dielectric stack structure.

	Proposed device	Control device
Gate electrode	Au	Au
Blocking layer	HfAlO (12 nm)	Al_2O_3 (12 nm)
Charge-storage layer	AlN (3 nm)	HfO_2 (3 nm)
Dual tunneling layer	HfON (2 nm)	Si_3N_4 (2 nm)
	SiO_2 (2 nm)	SiO_2 (2 nm)

p-type Si substrate with a resistivity of 5–10 Ω cm. Then, a 2-nm HfON was deposited by reactive sputtering of HfO_2 in an Ar/N_2 (24:6) ambient, followed by a deposition of a 3-nm AlN by reactive sputtering of Al in an Ar/N_2 (24:6) ambient, and then a deposition of a 12-nm HfAlO by reactive co-sputtering of HfO_2 and Al in Ar ambient. A post-deposition annealing (PDA) was carried out in N_2 at 700 °C for 60 s to improve the dielectric quality. For obtaining densification and high-quality tunneling layer and especially blocking layer, their deposition rates were set at a lower value of 0.125 nm/min and 0.1 nm/min respectively. On the contrary, the charge-storage layer was deposited at a higher rate of 2 nm/min so that more deep-level traps can be formed during deposition. For comparison, a normal high-k gate stack of $Au/Al_2O_3/HfO_2/(Si_3N_4/SiO_2)/Si$ (as control sample) was prepared using the same deposition procedure, with Si_3N_4 RF-deposited using Si_3N_4 target at a rate of 0.1 nm/min in Ar, HfO_2 RF-deposited using HfO_2 target at a rate of 0.17 nm/min in Ar, and Al_2O_3 RF-sputtered using Al target at a rate of 0.084 nm/min in Ar/O_2 (24/6) ambient. Each dielectric layer had the same physical thickness as the corresponding layer in the proposed device. For avoiding the crystallization of HfO_2, the PDA was performed at a low temperature of 500 °C for 120 s in N_2. Finally, high-work-function Au was evaporated and patterned as gate electrode and then Al was evaporated as back electrode, followed by forming-gas annealing which was completed in H_2/N_2 (5% H_2) for 20 min at 400 °C.

To examine the physical thickness of each dielectric layer and the interface quality between adjacent dielectric layers after the fabrication processes, transmission electron microscopy (TEM, Model: FEI Tecnai G2 20 Scanning TEM, operating voltage: 200 kV) was used to take cross-sectional images. For evaluating the memory window and programming/erasing characteristics, high-frequency (1-MHz) capacitor–voltage (C–V) curves were measured using HP4284A precision LCR meter at room temperature, and the programming/erasing voltages were applied by HP4156A precision semiconductor parameter analyzer.

3. Results and discussion

In Fig. 1(a) and (b), the schematic band diagrams of the two samples are compared. The values of the bandgap, ΔE_C and ΔE_V with respect to the conduction and valence bands of SiO_2 respectively are from Refs [11,18–20]. The ΔE_C of HfON is larger than that of Si_3N_4. The barrier height of HfAlO and the electron affinity of AlN can be adjusted by changing the Hf/Al ratio and Al/N ratio respectively, making them as promising materials for application in bandgap-engineered MONOS memory. For the proposed structure, the combination of AlN with high electron affinity [21] and HfAlO with appropriate Al content [12] could reach a good compromise in terms of thermal stability, dielectric constant and barrier height.

Fig. 2 shows the cross-sectional TEM image of the proposed gate stack structure. The clear interface between adjacent layers indicates that inter-diffusions between the layers can be effectively suppressed because the nitride (AlN) and oxynitride (HfON) layers located at the middle of the stacked gate dielectric can play a role of blocking impurity inter-diffusions due to nitrogen-related barrier [22,23]. From the TEM image, it can be clearly seen that the physical thickness of the

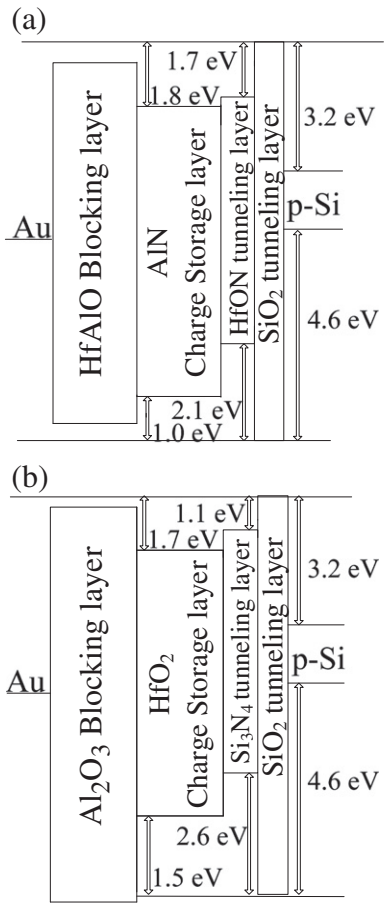

Fig. 1. Schematic band diagram of (a) the proposed structure of Au/HfAlO/AlN/(HfON/SiO_2)/Si and (b) the control structure of $Au/Al_2O_3/HfO_2/(Si_3N_4/SiO_2)/Si$.

stacked HfAlO/AlN/(HfON/SiO_2) is 12.5 nm/3.2 nm/(1.7 nm/2.0 nm) (an ultrathin DTL), very close to the design values, indicating the feasibility of sputtering and anneal processing for both the proposed device and the control device.

According to the physical thickness from TEM image and the relative permittivity of each dielectric layer in the proposed sample and control sample [12,21,24], the values of accumulation capacitance could be calculated to be 38 pF and 30 pF respectively, larger than the values extracted from the measured C–V curves of the two samples (31 pF and 25 pF respectively). This could be because the k values of the deposited dielectrics are smaller than those given in the above literature, due to the amorphous state of the films and difference in elemental composition. Based on the same reduction trend of accumulation capacitance of the two samples, it is believed that the values of accumulation capacitance are basically consistent with the dielectric thicknesses.

To study the quality of the HfON/SiO_2 and Si_3N_4/SiO_2 dual tunneling layers, MIS capacitors with HfON/SiO_2 and Si_3N_4/SiO_2 as gate dielectric were also fabricated under the same processing conditions as the two samples. Fig. 3 shows the C–V curve of the MIS capacitors swept in two directions under +/−8 V sweeping voltage. Small C–V hysteresis (<50 mV) is observed, indicating almost trap-free dual tunneling layers. Moreover, the elemental percentage is determined to be 53.5% for Al and 46.4% for O in the Al_2O_3 blocking layer by X-ray photoelectron spectroscopy, close to the stoichiometry of ideal Al_2O_3 (52.9% for Al and 47.0% for O).

The memory window is determined from the shift of the flat-band voltage, extracted from the measured C–V curves under different P/E voltages. As can be seen from Fig. 4, the memory window of the proposed device at P/E voltages of +8 V/−10 V, +8 V/−12 V,