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Effect of electrical and mechanical stresses of low temperature a-Si:H thin film transistors fabricated on polyimide and glass substrates

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ABSTRACT

Hydrogenated amorphous silicon thin film transistors (TFTs) were fabricated by plasma enhanced chemical vapor deposition on both transparent polyimide and glass substrate. The electrical characteristics and surface morphology of a-Si:H/SiN_x:H films on polyimide and glass substrate were compared. TFTs fabricated on polyimide substrate show better electrical performance than on glass substrate. Moreover, the threshold voltage shift of TFTs on polyimide substrate is smaller than those TFTs on glass. The similar trend is also found either under electrical stress or 0.2% mechanical strain. The superior electrical characteristics of TFTs on polyimide substrate than that on glass substrate were attributed to the better surface morphology of a-Si:H/SiN_x:H film on polyimide.

1. Introduction

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) fabricated on plastic substrates are attractive for flexible active matrix display [1,2]. Flexible displays have many advantages relative to the conventional glass based displays such as lighter and thinner as well as reduced incidences of breakage. The initial applications of flexible display are electronic papers, smart labels, sensor skins, curved displays, etc. The plastic substrate should be transparent for active-matrix liquid crystal displays or the bottom emitting active matrix organic light emitting display applications. The polyimide (PI) Kapton™ is typically used as plastic substrate for TFT fabrication. However, Kapton™ is not fully transparent and its color is orange-brown. A low transparent PI substrate can only be used in self-emitting or reflective displays. Therefore, the colorless PI substrate with a 40 μm-thick layer and an area of 18 cm × 18 cm was used in this study. In addition, the transmittance of the colorless PI substrate is 90% under visible light (λ = 550 nm).

The a-Si:H TFTs exhibit a metastable shift in threshold voltage when subject to prolonged gate bias. Many reports address the electrical stability of a-Si:H TFTs on the plastic substrate under flat status [3,4]. However, the electrical performance of the a-Si:H TFTs on plastic substrate under the strain status is very important for future flexible display application. In this work, the electrical performance of a-Si:H TFTs on PI (flat status), PI (under strain) and glass was studied. The electrical stress was performed at $V_{GS} = 20$ V and $V_{DS} = 15$ V, when the a-Si:H TFTs were used as switches in active matrix display.

2. Experimental details

Bottom-gate TFTs with a back-channel-etch structure were fabricated both on glass and PI substrates. The channel length was 8 μm and the channel width was 80 μm. The fabrication steps were as follows. First, a Ti/Al/Ti tri-metal layer with a total thickness of 200 nm was deposited by sputtering and then patterned by dry etching to form the gate electrodes. The opposite stresses of Ti and Al can eliminate their internal stress, thus preventing the delamination of metal electrodes from the PI substrate. Second, silicon nitride, a-Si:H, and n+ a-Si:H were deposited sequentially by 13.56 MHz RF plasma-enhanced chemical vapor deposition at 200 °C. The thicknesses of the SiN_x, a-Si:H, and n+ a-Si:H layers were 300, 200, and 50 nm, respectively. Third, an active island of n+ a-Si:H/a-Si:H layer was formed by the island-etching process. The source/drain metals were deposited and then defined by dry etching to form the source/drain electrodes. Finally, the n+ layer region between the source and drain electrodes was etched away.

Silicon nitride films were deposited from a mixture of $SiH_4/NH_3/N_2/H_2$ gases (40/148/650/700 sccm), and the working pressure was set at 9×10^{-1} Torr at the RF power of 340 W (power density = 1.73×10^2 mW/cm^2). The a-Si:H films were deposited from a mixture of SiH_4/H_2 gases (50/450 sccm), and the working pressure was set at 7.5×10^{-1} Torr. A lower RF power of 30 W (power density = 1.73×10^2 mW/cm^2) was used to avoid the plasma damage in the active layers. Moreover, phosphine was used as a dopant source during n+ layer deposition. The surface morphology and roughness of the films were measured by field emission scanning electron microscope (FE-SEM) (JEOL JSM-7000F), at the operating voltage of 15 kV and atomic force microscopy (AFM) (Veeco DI-3100), in non-contact mode, respectively. The field effect mobility and threshold voltage

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of devices were calculated from the current–voltage characterization by an HP-4156C semiconductor parameter analyzer. Moreover, an HP-4284A capacitance–voltage (C–V) meter was used for C–V measurement of a-Si:H TFTs at room temperature.

3. Results and discussion

Fig. 1(a) and (b) reveals the FE-SEM observation of the a-Si:H/SiN_x:H film deposited on the glass and PI substrates, respectively. Several microcracks are observed for the a-Si:H/SiN_x:H film on glass. Based on this observation, it is believed that the film stress must be considered. It has been known that the residual stress of thin films contains both intrinsic and extrinsic stress. Intrinsic stress of thin film depends on the chemistry, microstructure, and particle bombardment. Extrinsic stress is commonly applied to the film by the difference in thermal expansion coefficient between the film and the substrate [5]. During deposition, the intrinsic stress is induced by ion bombardment. A large intrinsic stress can be found for the substrate with a high Young's modulus. It has been known that the Young's modulus of the glass and PI are 50 and 2.5 GPa, respectively. Hence, the intrinsic stress of a-Si:H/SiN_x:H films on the glass is larger than that on the PI. On the other hand, the thermal stress (extrinsic stress) is also considered. This is because the as-deposited a-Si:H/SiN_x:H films on the glass and PI substrates were cooled down from 200 °C to the room temperature immediately in this work, which is similar to the mass production line in factory. It has been known that the coefficients of thermal expansion (CTE) of glass and colorless PI are 10 and 17 ppm/°C, respectively [6]. After deposition process, the induced thermal stress of the film on the PI is slightly larger than that on the glass. Therefore, the major residual stress of the film is from intrinsic stress and causes the a-Si:H/SiN_x:H film on the glass to have several microcracks. Based on the fracture mechanics for thin film, the relation between residual stress, σ_R and stress intensity factor, K_c is given by [7]

$$K_c = \sigma_R \sqrt{Zd}, \tag{1}$$

where Z is constant, which is described by Hutchinson and Suo [8] and d is the film thickness. When the stress intensity factor exceeds a critical value, K_{IC}, the microcrack grows catastrophically and failure occurs. Hence, the origin of the microcracks on the a-Si:H/SiN_x:H/glass is attributed to the residual stress release. However, the as-deposited a-Si:H/SiN_x:H film on glass cooled down to the room temperature in vacuum is found in many works. This end step is like the annealing process, and then the microcrack is not obvious. The root mean square surface roughnesses of the a-Si:H/SiN_x:H film on glass and on PI substrates measured by AFM are 6.64 and 1.64 nm, respectively. Taking 180 MPa and 40 MPa compressive residual stresses for a 300 nm SiN_x:H film on the glass and PI substrates [9,10], and Z = 1.976 for channel cracks [8] into Eq. (1), gives 0.138 and 0.031 MPa·$m^{1/2}$, respectively. The K_c difference is great, because the Young's modulus of the PI substrate is 20 times smaller than that of the glass and causes the film microcrack on the glass. This result is consistent with the SEM observation.

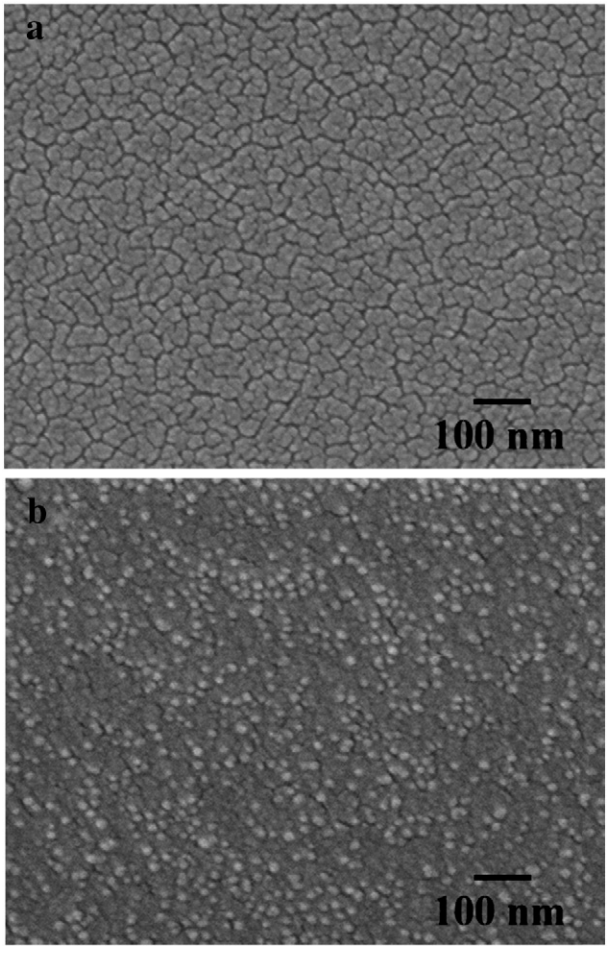

Fig. 1. (a) Transfer characteristics and (b) output characteristics of the a-Si:H bottom-gate TFT fabricated on the glass substrate.

Fig. 2(a) and (b) shows the transfer and output characteristics of an a-Si:H bottom-gate TFT fabricated on a glass substrate, respectively. The on/off drain current ratio at $V_d = 10$ V is greater than 10^7. This is due to the higher on-state and lower off-state leakage currents for the high-quality a-Si:H and SiN_x:H films. The hydrogen content in a-Si:H layer is 5×10^{21} atoms/cm^3 from secondary ion mass spectrometry, which is greater than that of the conventional a-Si:H. The larger hydrogen content in the a-Si:H film is due to the less thermal evolution process at a low temperature. The hydrogen in the amorphous silicon film can passivate the defects by forming a Si – H bond. As the hydrogen content of the a-Si:H film is increased, the number of dangling bonds is reduced. Therefore, the performance of a-Si:H TFTs can be improved by applicable hydrogen content to passivate the defects. Moreover, the breakdown voltage of the SiN_x:H film is about 8 MV/cm from a metal/insulator/metal structure measurement. The gate-to-source leakage current (I_{gs}) is around 10^{-13} A. It indicates the superior quality of the a-SiN_x:H layer. The field effect mobility and the subthreshold voltage swing were measured at the V_{DS} of 0.1 V and the values were 0.35 cm^2 V^{-1} s^{-1} and 0.52 V/dec, respectively. This mobility of a-Si:H TFT on the glass is close to the other works, which reports in the range of 0.1 to 0.7 cm^2V^{-1} s^{-1} for the V_{DS} of 0.1 V [11,12]. The output characteristic shows no current crowding effect at low V_d and no kink current effect at high V_d because of the low resistivity of the ohmic contacts and low defect density in the a-Si:H film.

Fig. 3(a) and (b) shows the transfer and output characteristics of an a-Si:H bottom gate TFT fabricated on a PI substrate, respectively. The electrical characteristics of the TFT on the PI substrate are similar to those on the glass substrate. It also has a high on/off drain current ratio and a low gate-to-source leakage current, as shown in Fig. 3(a). This means that a high quality n+ a-Si:H/a-Si:H/SiN_x:H trilayer film was obtained on the PI substrate. The carrier mobility between the TFT on the glass and PI substrates is slightly different. The field-effect mobility of the TFT on the PI substrates is 0.49 cm^2 V^{-1} s^{-1}, which is higher than that on the glass substrate owing to the smoother surface roughness of the a-Si:H/SiN_x:H film on the PI substrate. It is noticed that the measured mobility of TFT on the glass and PI is the average value extracted from the nine TFT devices on the same substrate. The specific capacitance of the gate dielectric is 20 nF/cm^2 for a-Si:H TFTs on the glass and PI substrates. It has been known that the phonon,