



Light extraction efficiency improvement in GaN-based blue light emitting diode with two-dimensional nano-cavity structure

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ABSTRACT

The light extraction efficiency of light emitting diode (LED) devices was improved by embedding nano-sized two-dimensional, air cavity photonic crystal (PC) structure on the indium tin oxide (ITO) layer of GaN-based LEDs. The embedded air cavity PC structure was fabricated using a reversal imprint lithography technique. The nano-cavity patterns had a width of 560 nm, a space of 240 nm and a height of 280 nm. According to current–voltage characterization, the electrical performance of the LED devices was not degraded by the fabrication process of air cavity PC structure. The optical output power of the LED device was increased by up to 10% at a drive current of 20 mA by forming the nano-cavity PC structure on the transparent electrode of the blue LED device, which was grown on a patterned sapphire substrate, to maximize the photon extraction. Since photons are scattered with cavities and are unaffected by the packaging process, which is the encapsulation of a LED device with epoxy resin, this enhancement in light extraction efficiency will not be decreased after the packaging process.

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1. Introduction

Light emitting diodes (LEDs) have become one of the most promising for next generation lighting sources due to their low power consumption, long life-time, small form factor, and eco-friendly nature [1]. The industrial need for high brightness LEDs is rapidly increasing. On the other hand, no LED has sufficient efficiency to build high brightness LEDs. Among the factors affecting the efficiency loss of LEDs, one of the largest is the total internal reflection (TIR) inside the device [2]. Total internal reflection inevitably originates from the large difference in refractive index between the LED structure and outer ambient [3]. Conventional GaN-based LEDs have low light extraction efficiency because most of the light emitted from active layer is trapped inside the GaN crystal by total internal reflection. To construct high brightness LEDs, the low external light extraction efficiency of the LED needs to be improved. Accordingly, many studies, such as those on surface roughening [4,5], the insertion of reflector [6], the formation of a photonic crystals (PC) structure [7,8], the moth-eye structure [9], and LEDs grown on patterned sapphire substrates [10,11], have been made to enhance the light extraction efficiency by suppressing the total internal reflection. A two-dimensional (2-D) PC slab was importantly examined due to its large enhancement effect of light extraction of LEDs. However, it is common that the process of fabricating a PC structure on the LED structure involves the plasma-based etching

process. If plasma-based dry etching process was induced inside the LED structure, such as indium tin oxide (ITO) or p-GaN layer, electrical property of the LED devices could be degraded [12–14]. Therefore, a technique of fabricating 2-D PC structures on LED devices without a plasma-based etching process needs to be developed to apply the 2-D PC structure to LED devices.

This paper reports an enhancement of the light extraction efficiency by forming a two-dimensional air cavity PC structure on the ITO layer of GaN-based LEDs. The light extraction efficiency of the LEDs can be improved by the air cavity PC structure. Since the fabrication of air cavity PC structure does not employ plasma-based dry etching process, the electrical properties of the LED device was not degraded. In addition, the enhancement of the light extraction efficiency due to the air cavity PC structure will not be decreased after the packaging process, which is the encapsulation of a LED device with epoxy resin.

2. Experiments

2.1. Fabrication of the LED devices

The GaN-based blue LED was grown by a conventional metal organic chemical vapor deposition (MOCVD) process on a c-plane sapphire substrate with a few micro-sized surface protrusion patterns. This blue LED device consisted of a 5 μm un-doped GaN layer, a 3 μm n-GaN layer, five pairs of In_{0.15}Ga_{0.85}N/GaN multiple quantum well layers, and a 100 nm p-GaN layer, which were all stacked together. After the MOCVD growth process, a 220 nm thin ITO layer was sputtered onto the p-GaN layer as a current spreading layer. The

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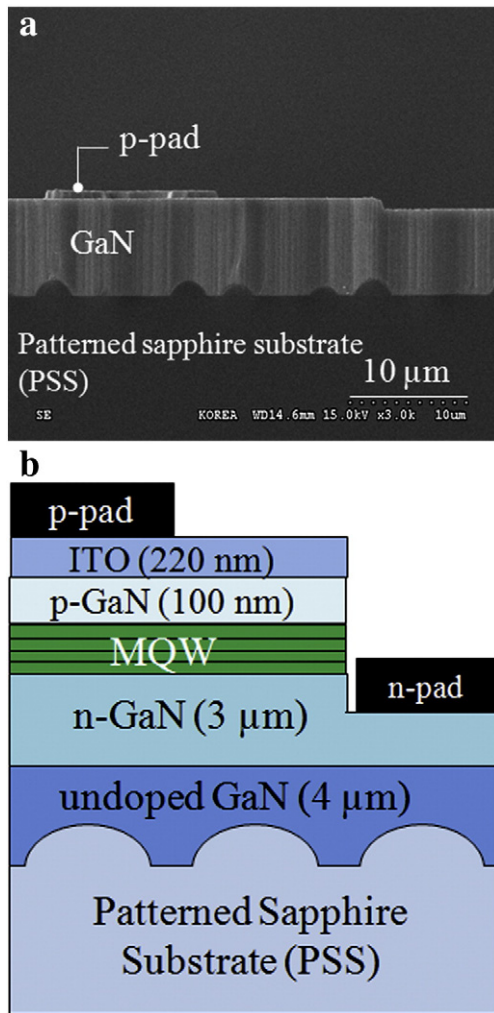


Fig. 1. SEM image of the fabricated LED devices: (a) Cross-sectional image and (b) schematic diagram of structure of fabricated LED devices.

weight ratio of $\text{In}_2\text{O}_3:\text{SnO}_2$ in the sputtered ITO layer was approximately 85:15. In this study, $300 \times 300 \mu\text{m}$ LED chips were fabricated by conventional photolithography and an etching process. Initially, the photoresist pattern for mesa structures was formed on the ITO layer using photolithography. The ITO layer was then etched using a wet chemical solution, and the underlying GaN layer was etched using an inductive coupled plasma etching process with Cl_2 -based plasma. After the etching process, mesa photoresist patterns were removed. This was followed by the photolithography for p- and n-electrode patterns and the deposition of Cr/Au (50/500 nm) on the n-GaN layer as an n-pad electrode and on the ITO layer as a p-pad electrode by electron-beam evaporation [15]. LED devices were then subsequently rapid thermal annealing (RTA) under flowing N_2 at temperatures 350°C for 1 min for p- and n-electrode. The structure of the fabricated LED device was confirmed by field emission scanning electron microscopy (FE-SEM, Hitachi S-4300, operated at 15 kV). Fig. 1(a) and (b) show the SEM image and schematic diagram of the structure of the fabricated LED device, respectively. As shown in Fig. 1, the LED structure was formed on a patterned sapphire substrate.

2.2. Fabrication of the embedded 2-D nano-cavity, air-void PC structure on the LED devices

Fig. 2 describes that the overall fabrication process of the air cavity PC structure on an ITO electrode layer of LEDs. First, the polymer PC structure was fabricated using UV-curable nano-imprint lithography. A polyvinyl alcohol (PVA) layer, which is a water-soluble material, was spin-coated on a polyethyleneterephthalate (PET) film prepared at a rotational speed of 1000 rpm for 30 sec. The PET film, which was used as the supporting layer, helps facilitate the UV-curable nano-imprint process. A methacryloxypropyl-terminated polydimethylsiloxane (m-PDMS)-based UV-curable liquid-phase imprint resin was then dispensed on the Si master template. As a master template for the UV-curable nano-imprint process, the Si master template with a nano-pillar array, which had a diameter of 300 nm, a pitch of 600 nm and height of 220 nm, was used. The Si master template was fabricated using the electron-beam lithography and reactive ion etching process with

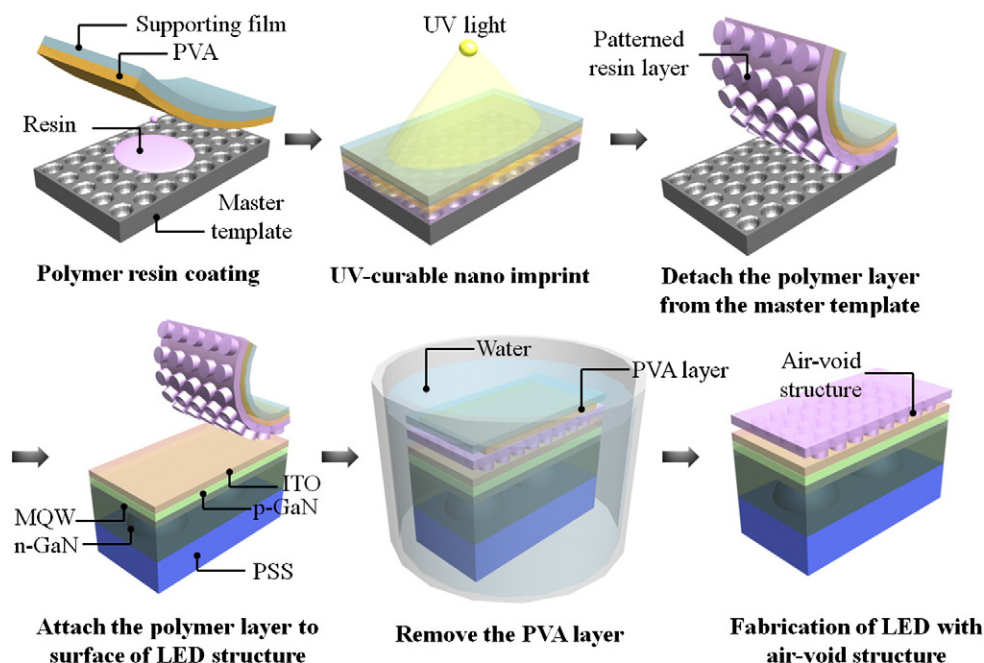


Fig. 2. Schematic diagram of air-void PC structure fabrication process.

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