Thin Solid Films 521 (2012) 168–171

Contents lists available at SciVerse ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

High-performance InGaP/GaAs superlattice–emitter bipolar transistor with multiple S-shaped negative-differential-resistance switches under inverted operation mode

Jung-Hui Tsai [a], Chia-Hong Huang [a], Wen-Shiung Lour [b], Yi-Ting Chao [a], Jhih-Jhong Ou-Yang [a], Jia-Cing Jhou [a,*]

[a] Department of Electronic Engineering, National Kaohsiung Normal University, 116 Ho-ping 1st Road, Kaohsiung 802, Taiwan
[b] Department of Electrical Engineering, National Taiwan Ocean University, 2 Peining Road, Keelung 202, Taiwan

ARTICLE INFO

Available online 8 January 2012

Keywords:
Superlattice emitter
Pseudomorphic base
Negative-differential-resistance
Turn-on voltage
Avalanche multiplication
Confinement effect

ABSTRACT

Based on the employments of an InGaP/GaAs superlattice emitter and a thin InGaAs pseudomorphic base structure, the device with excellent transistor action and multiple S-shaped negative-differential-resistance (NDR) switching behavior are achieved. Under normal transistor operation mode, the tunneling electrons could easily transport from InGaP/GaAs superlattice over the n-GaAs emitter layer into the thin InGaAs pseudomorphic base region for reducing the base–emitter turn-on voltage and promoting the current gain. In particular, an interesting multiple S-shaped NDR behavior is observed under inverted operation mode due to the avalanche multiplication and confinement effect for electrons at the interface between superlattice and emitter layer, respectively. As an appropriate voltage source and a load resistor are applied, three stable operation points are obtained.

1. Introduction

Heterojunction bipolar transistors (HBTs) fabricated by III–V compound semiconductors had attracted considerable interest in high-speed digital circuit applications due to the superior performance [1, 2]. However, the conventional HBTs suffered from a large collector–emitter (C–E) offset voltage (ΔV_{CE}) resulting from the difference of turn-on voltages between base–emitter (B–E) and base–collector (B–C) junctions. It will cause unnecessary power consumption in signal amplification application [3, 4]. Previously, GaAs based HBTs utilizing a small energy-gap InGaAs ternary alloys material as base layer is an improved method to decrease the B–E turn-on voltage and C–E offset voltage [5]. However, the thickness of InGaAs base layer is limited due to the lattice mismatch with GaAs material.

On the other hand, switching devices exhibiting N or S-shaped negative-differential-resistance (NDR) characteristics had been widely used in high-speed switches and high-frequency oscillators [6–11]. In general, the S-shaped NDR devices, e.g., bulk barrier switches, only provide two stable operation regions, i.e., initial off and final on states. In order to obtain more stable operation points for multiple-value logic circuit application, the research and development of multiple S-shaped NDR devices are considerably important.

In this article, the performance of a functional InGaP/GaAs superlattice–emitter HBT (SEHBT) employing a thin InGaAs pseudomorphic base layer is experimentally demonstrated. Excellent transistor characteristics are obtained under normal operation mode and an interesting two-route S-shaped NDR behavior is observed under inverted operation mode, respectively. The SEHBT/NDR combining devices can greatly

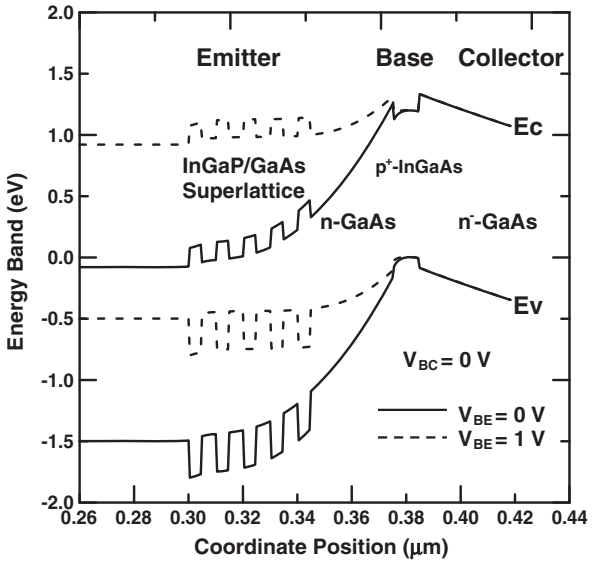

Fig. 1. Corresponding energy band diagrams near base–emitter junction of the SEHBT at equilibrium and $V_{BE} = 1.0$ V, respectively.

* Corresponding author. Fax: +886 7 6051330.
E-mail address: jhtsai.jhtsai@msa.hinet.net (J.-C. Jhou).

0040-6090/$ – see front matter © 2012 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2011.12.082

reduce the number of elements and process steps, and could provide great design flexibility in circuit applications.

2. Experiments

The studied functional SEHBT was grown on an (100) oriented semi-insulating GaAs substrate by low-pressure metal–organic chemical-vapor deposition system. The epitaxial layers consisted of a 0.5 μm $n^+ = 1\times 10^{19}\,cm^{-3}$ GaAs subcollector layer, a 0.5 μm $n^- = 2\times 10^{16}\,cm^{-3}$ GaAs collector layer, a 100 Å $p^+ = 1\times 10^{19}\,cm^{-3}$ $In_{0.15}Ga_{0.85}As$ base layer, a 300 Å $n = 5\times 10^{17}\,cm^{-3}$ small energy-gap GaAs emitter layer, and an $n = 5\times 10^{17}\,cm^{-3}$ $In_{0.49}Ga_{0.51}P$/GaAs superlattice layer. Finally, a 0.3 μm $n^+ = 1\times 10^{19}\,cm^{-3}$ GaAs cap layer was deposited on the superlattice. The superlattice structure included five-period 50 Å $In_{0.49}Ga_{0.51}P$ layers and four-period 50 Å GaAs layers. Trimethylindium, trimethylgallium, phosphine (PH_3), and arsine (AsH_3) were used as the In, Ga, P, and As sources, respectively. The dopants used for n and p layers were silane (SiH_4) and dimethylzine, respectively. After the epitaxial growth, the conventional photolithography, vacuum evaporation, and wet selective etching processes were used to fabricate the device. In particular, due to the thin thickness of the base layer, the patterned V-grooves were etched through the p^+-$In_{0.15}Ga_{0.85}As$ base layer into the n^--GaAs collector layer. Ohmic contact was formed by alloying AuGeNi metal for n-type emitter and collector. AuZn metal was deposited on the V-grooves to facilitate the p-type ohmic contact. The emitter area is $50\times 50\,\mu m^2$.

3. Experimental results and discussion

The energy band diagrams near the B–E junction of the studied SEHBT at equilibrium and under normal operation mode are illustrated in Fig. 1. Obviously, the potential spike at B–E junction is completely eliminated, even at $V_{BE} = 1.0$ V. This condition can be attributed that the use of a thin n-GaAs emitter layer between superlattice and base layer could help to lower the energy band at emitter side and eliminate the potential spike. Fig. 2(a) shows the common-emitter current–voltage (I–V) characteristics at room temperature. It exhibits a maximum collector current of 91 mA and a maximum current gain of about 580. The enlarged view near the origin of the I–V characteristics is illustrated in Fig. 2(b). A relatively low ΔV_{CE} of only 31 mV at base current of 20 μA is observed. The low offset voltage can be attributed that (i) the potential spike has been completely eliminated to reduce the B–E turn-on voltage, and (ii) the B–E and B–C junctions are nearly symmetric homojunctions. Under normal transistor operation mode, part of the injecting electrons by tunneling behavior could easily transport over the small energy-gap GaAs emitter layer from the superlattice to decrease the neutral-emitter recombination current, as compared with the conventional HEBTs [12]. Furthermore, the "effective" valence band discontinuity at B–E junction could be enhanced for the use of a thin InGaAs pseudomorphic base layer, and it is approximately equivalent to the summation at $In_{0.49}Ga_{0.51}P$/GaAs and $In_{0.15}Ga_{0.85}As$/GaAs interfaces [13], which can provide good confinement effect for holes to promote the emitter injection efficiency. Also, the bulk-base recombination current of the traditional HBTs with a thick base layer can be reduced to increase the current gain.

When the base terminal is open, the two-terminal I–V characteristics under inverted operation mode at room temperature are revealed in Fig. 3. Clearly, an interesting two-route S-shaped NDR behavior is observed. The corresponding switching parameters, such as switching voltages $V_{S1} = 3.83$ V and $V_{S2} = 3.19$ V, holding voltages $V_{H1} = 3.36$ V and $V_{H2} = 2.80$ V, holding currents $I_{H1} = 1.96$ mA and $I_{H2} = 5.15$ mA,

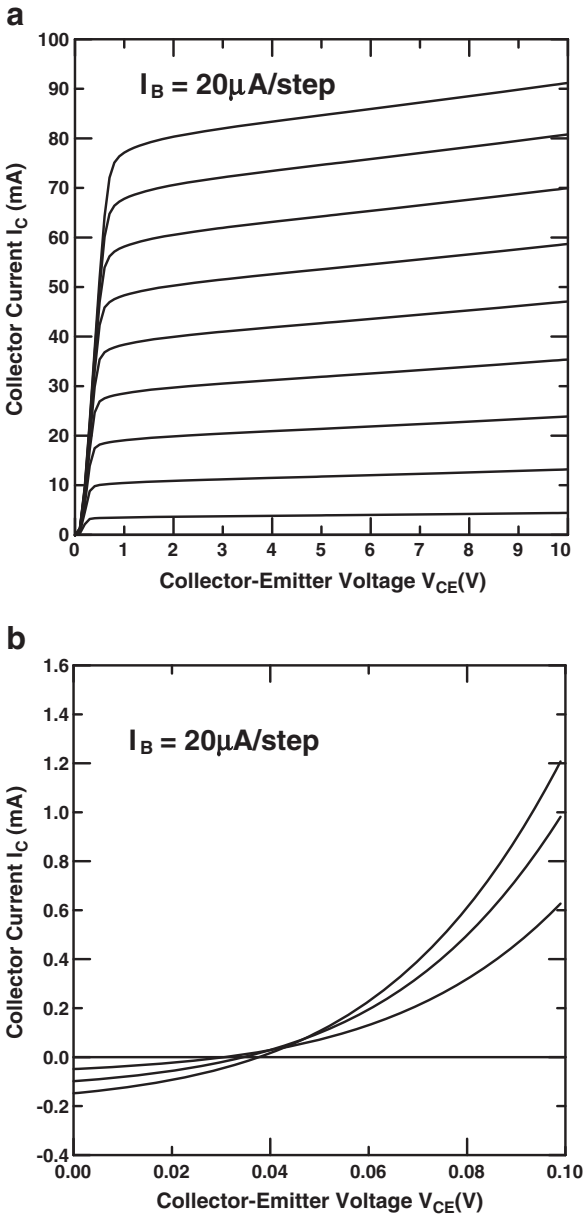

Fig. 2. (a) Common-emitter current–voltage characteristics of the studied device at room temperature. (b) Enlarged view near the origin of the current–voltage characteristics.

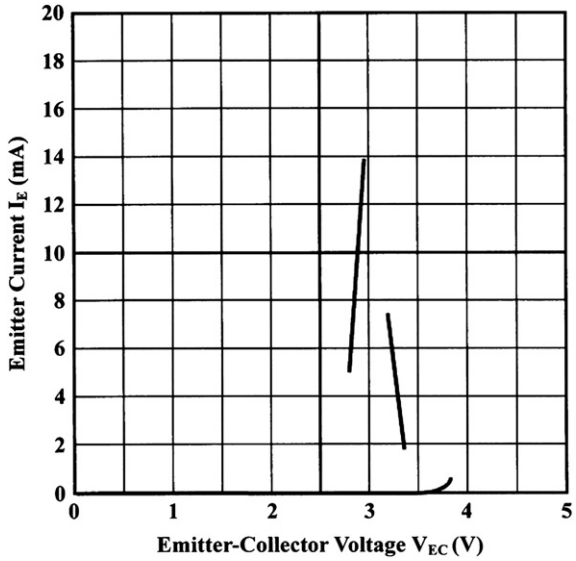

Fig. 3. Two-terminal current–voltage characteristics of the studied device under inverted operation mode at room temperature.