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Introduction of zirconium oxide in a hardmask concept for highly selective patterning of scaled high aspect ratio trenches in silicon

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ABSTRACT

The fabrication of high aspect ratio silicon trenches (critical dimension < 100 nm, aspect ratio > 10:1) by dry etch processing has proven to be a challenge mainly due to limited etch selectivity of conventional hardmask materials to Si. Moreover, for future technology nodes the hardmask thickness will be limited by the thickness of the photoresist. This work focuses on a concept to enable the usage of very thin resist layers (< 100 nm) for patterning of silicon trenches by the integration of an unconventional hardmask stack consisting of SiO_2 and ZrO_2. Deposition of such material films has been investigated, as well as e-beam lithography exposure and finally pattern transfer by dry etching. Using this hardmask stack and 100 nm thin resist, the fabrication of 35 nm wide trenches with an aspect ratio of ~20:1 is demonstrated revealing a very high selectivity (> 100:1) of the ZrO_2 layer to Si during the deep silicon etch. A silicon etch rate > 1.5 μm/min was achieved. The ZrO_2 layer itself provides the main selectivity improvements of the final hardmask stack.

1. Introduction

Zirconium oxide (ZrO_2) has been investigated in the last 10 years as gate dielectric material for metal–oxide–semiconductor field effect transistors [1–5] and as storage capacitor dielectric for dynamic random access memories (DRAM) [6]. Due to its adequate electrical properties, thermal stability and well understood integration behavior it is now widely used in DRAM fabrication. On the other hand, besides its electrical performance, ZrO_2 shows also a higher dry etch stability in comparison to more common dielectric materials such as Si_3N_4 or SiO_2. Therefore, in this paper ZrO_2 is used as a highly etch resistant dry etch hardmask (HM) especially for the fabrication of high aspect ratio trenches in silicon, where emerging thin resist technologies and thin hardmask technologies are required [7]. The patterning of high aspect ratio silicon structures is challenged by limited selectivities of the resist and conventional hardmask materials (e.g. C, SiO_2, SiON, Si_3N_4) to silicon. The reduction of the resist thickness is mainly driven by the decreasing depth-of-focus (DOF) in optical lithography that is using projection lenses with higher and higher numerical aperture (NA). Even though NA is more relaxed for extreme ultra violet (EUV) lithography DOF stays small because of the extremely small EUV wavelength. Another driver to reduce the resist thickness is the maximum aspect ratio (AR) of about 3:1 (AR = depth:width) due to pattern collapse [8]. Therefore the introduction of an efficient hardmask material with high etch resistance is a desirable approach to enable structuring of silicon structures with high aspect ratios for future technology nodes. This work focuses on the feasibility of a material stack of a thin SiO_2 layer and ZrO_2 as a hardmask stack to enable thin resist technologies including the investigation of stack deposition, the exposure of a thin resist mask using e-beam lithography as well as pattern transfer by dry etching.

2. Experimental details

2.1. Preparation of hardmask stack

The hardmask stack consisting of thin layers of 20 nm SiO_2 on 35 nm ZrO_2 was deposited on 300 mm Si wafers by Atomic Layer Deposition (ALD) using a single wafer reactor (Jusung Eureka 3000). The 20 nm SiO_2 film supports the pattern generation by dry etch processing enhancing the selectivity compared to pure resist to open the ZrO_2 layer. Furthermore the SiO_2 layer creates a more favorable surface for lithography than a crystalline and rough ZrO_2 film. The ZrO_2 was grown using TEMAZr (Tetrakis[ethylmethylamino] zirconium) which was supplied by direct liquid injection into a vaporizer, while ozone was used as oxidant. The deposition temperature was varied between 225 and 275 °C to verify growth in the ALD window of TEMAZr, i.e. a growth rate which is independent of the deposition temperature. The subsequent thin SiO_2 film was deposited using 3DMAS (Tris [dimethylamino]silane) and ozone. The silicon oxide deposition was

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performed on the same chamber as the ZrO_2 at a deposition temperature of 275 °C. The film thicknesses after deposition were measured using spectral ellipsometry (KLA TENCOR Spectra CD100). Additionally surface morphology and roughness of as deposited layer was characterized by means of atomic force microscopy (VEECO X3D). The AFM images were recorded on a scan area of 1 μm × 1 μm using TESPA tips in tapping mode.

2.2. Patterning of high aspect ratio trenches

The pattern generation flow starts with the exposure of the photo resist by lithography followed by dry etch processing to open the hardmask and finally to transfer the structures into the Si substrate. Hole and trench patterns were printed on 300 mm wafers using a Vistec SB3050DW shaped electron beam direct writer (50 kV acceleration voltage). A commercially available chemically amplified e-beam resist (p-CAR, positive tone) was spin coated, baked and developed on a resist track (CLEAN TRACK ACT12, Tokyo Electron Ltd.) with a thickness of about 100 nm (measured after development in 2.38% TMAH). The chemical composition of this e-beam resist is comparable to state of the art (PHOST-based) deep ultraviolet (DUV) or extreme ultraviolet (EUV) photo resists and shows therefore a similar etch resistivity. Critical dimensions (CD) of the printed patterns were measured and imaged using a CD scanning electron microscope (VeritySEM 4i®, Applied Materials) operated at 3.5 kV.

The dry etching of the hardmask stack was performed at two different industrial 300 mm capacitive coupled plasma source etch chambers. The

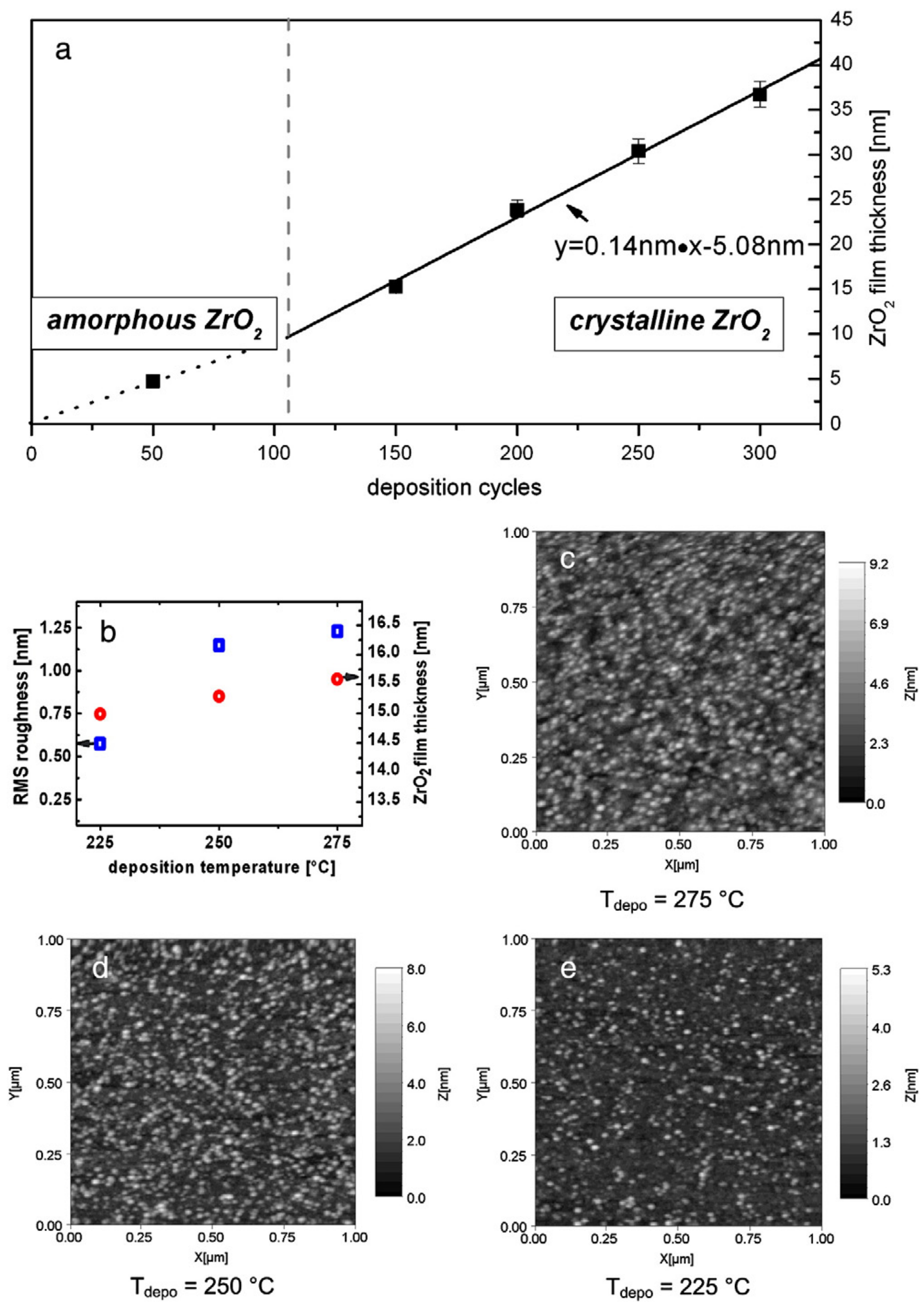

Fig. 1. a) Growth rate for ZrO_2 films deposited at 275 °C and b)–e) thickness and roughness dependency of ZrO_2 film (150 cycles) deposited at different temperatures.