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Critical review

Review of recent developments in amorphous oxide semiconductor thin-film transistor devices

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ABSTRACT

The present article is a review of the recent progress and major trends in the field of thin-film transistor (TFT) research involving the use of amorphous oxide semiconductors (AOS). First, an overview is provided on how electrical performance may be enhanced by the adoption of specific device structures and process schemes, the combination of various oxide semiconductor materials, and the appropriate selection of gate dielectrics and electrode metals in contact with the semiconductor. As metal oxide TFT devices are excellent candidates for switching or driving transistors in next generation active matrix liquid crystal displays (AMLCD) or active matrix organic light emitting diode (AMOLED) displays, the major parameters of interest in the electrical characteristics involve the field effect mobility (μ_{FE}), threshold voltage (V_{th}), and subthreshold swing (SS). A study of the stability of amorphous oxide TFT devices is presented next. Switching or driving transistors in AMLCD or AMOLED displays inevitably involves voltage bias or constant current stress upon prolonged operation, and in this regard many research groups have examined and proposed device degradation mechanisms under various stress conditions. The most recent studies involve stress experiments in the presence of visible light irradiating the semiconductor, and different degradation mechanisms have been proposed with respect to photon radiation. The last part of this review consists of a description of methods other than conventional vacuum deposition techniques regarding the formation of oxide semiconductor films, along with some potential application fields including flexible displays and information storage.

Contents

1. Introduction

Since the demonstration of flexible amorphous In–Ga–Zn–O (indium gallium zinc oxide, IGZO) thin-film transistors (TFTs) by Nomura et al. in 2004 [1], tremendous efforts have been made in

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amorphous oxide semiconductor (AOS) TFT device research, especially for next generation flat panel display (FPD) applications. Compared to amorphous silicon (a-Si), TFT devices that act as switching transistors in active matrix liquid crystal displays (AMLCD), which typically exhibit field effect mobility values lower than 1 cm^2/Vs [2–4], much higher electrical performance can be achieved using n-type oxide semiconductors, with practical field effect mobility values exceeding 5 cm^2/Vs.

The major advantage of oxide semiconductor materials is that they can be deposited using conventional semiconductor process methods such as sputtering at room temperature, and their amorphous structure enables the realization of uniform device properties over large areas. Because of such remarkable characteristics, oxide semiconductor TFTs are excellent candidate switching elements for large area (>70 in.), ultra definition (UD, 4000×2000), and fast frame rate (>240 Hz) AMLCD panels. By properly implementing IGZO TFT arrays, Samsung Electronics successfully developed a 70-inch 240 Hz 3D UD TV prototype that was presented at FPD International 2010 in November [5].

In addition to AMLCDs, oxide semiconductor TFTs are also promising alternatives to low temperature poly-silicon (LTPS) TFTs that are used as driving elements in active matrix organic light-emitting diode (AMOLED) displays. Despite the high electrical performance of LTPS TFTs that exhibit typical field effect mobility values close to 100 cm^2/Vs, the non-uniform spatial distribution of poly-Si grain structure in LTPS films results in non-uniform device properties over large areas, which is the reason why current AMOLED displays are limited to relatively small size applications such as mobile cell phones. Accordingly, several companies have demonstrated working prototype AMOLED panels driven by AOS TFTs [6–8].

Amorphous oxide semiconductor devices have thus been drawing worldwide attention during the past few years, and display companies are now very close to achieving mass production of commercial products that integrate AOS TFT backplanes. In that regard, the present article aims at providing a review on the recent development of AOS TFT devices and the major issues that need to be addressed in order to succeed in the transition from basic research to product generation. The first section consists of an overview on the enhancement of device performance. The electrical characteristics of TFT devices are represented by the field effect mobility (μ_{FE}), threshold voltage (V_{th}), and subthreshold swing (S). Such parameters strongly depend on the device structure and fabrication process, the AOS materials, and the gate dielectrics or interconnect metals in contact with the semiconductor. Because fast switching is the key role of TFT devices in electronic applications, one would in general target high μ_{FE} values, V_{th} close to zero, and SS values as small as possible.

The next section discusses reliability issues concerning AOS TFT devices. As the pixel TFTs in AMLCD or AMOLED panels in operation constantly undergo either gate bias stress or constant current stress, it is important to understand the behavior of the devices under such stress conditions. The associated device degradation usually occurs in the form of V_{th} shifts, which are occasionally accompanied by severe losses in field effect mobility. In order to promote reasonable product lifetime in display panels, it is thus imperative to minimize the susceptibility of AOS TFTs with respect to voltage or current stress.

The last section presents methods other than conventional vacuum deposition techniques for the formation of AOS thin films. Solution-based processes are reviewed, and some potential applications where the integration of AOS TFTs may be effective are discussed, including flexible electronics and information storage.

2. Optimization of AOS TFT device performance

The electrical characteristics which determine device performance are evaluated in terms of several parameters such as field effect mobility (μ_{FE}), threshold voltage (V_{th}), and subthreshold swing (S). These parameters are in general extracted in compliance with the gradual channel approximation. By measuring the drain current (I_{DS}) with respect to gate voltage (V_G), the mobility can be obtained from Eq. (1),

$$I_{DS} = \frac{W}{L}\mu C_i\left[(V_G - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right], \quad (1)$$

where μ denotes the mobility in the channel, V_{th} the threshold voltage, and V_G the applied gate voltage. V_{DS} is the source-drain voltage, and C_i is the capacitance of the gate insulator per unit area.

The saturation mobility (μ_{sat}) is obtained from I_{DS} in the saturation regime under the condition $V_{DS} \gg (V_G - V_{th})$ using the following equation:

$$I_{DS}^2 = \sqrt{\frac{W}{2L}\mu C_i}(V_G - V_{th}). \quad (2)$$

In the small V_G regime (linear region), the mobility is defined as the linear field-effect mobility. Generally, I_{DS}–V_G curves are nonlinear, so the maximum value of μ_{FE} is often reported. The apparent field-effect mobility induced by the transconductance g_m at a low drain voltage is determined by

$$\mu_{FE} = \frac{Lg_m}{WC_iV_{DS}}. \quad (3)$$

Another important TFT parameter is the subthreshold swing (S), which reflects the amount of V_G change required to increase I_{DS} by an order of magnitude in the subthreshold region. From the transfer characteristics, S can be extracted using the equation:

$$S = \frac{dV_S}{d(\log_{10} I_{DS})}. \quad (4)$$

The S value also provides important information about the quality of a TFT. It is related to the total trap density N_t near the semiconductor/gate dielectric interface by:

$$N_t = \left[\frac{S\log(e)}{kT/q} - 1\right]\frac{C_i}{q}. \quad (5)$$

Here, k is the Boltzmann constant and q is the charge of an electron.

2.1. Device structure

Fig. 1 illustrates typical device structures that are adopted in the fabrication of amorphous oxide semiconductor TFTs. The TFT structure can be specified by the stacking order of the gate, oxide semiconductor, and source/drain electrodes. They can be classified more precisely into combinations of top/bottom gate and top/bottom contact. The top-gate structure was employed to fabricate devices with epitaxial semiconductor layers, for which it is difficult to form bottom electrodes [9]. This structure has another advantage in that the upper gate insulator and electrodes may act as a passivation, which protects the channel layer from external damage. The top gate structure was studied in the early stage of oxide semiconductor research owing to simple fabrication methods that involve as few as two patterning mask steps [1,10]. Top gate structures were then studied to enhance the device performance by reducing the parasitic capacitance [11] and the photosensitivity with respect to light emanating from the upper OLED [12].

Meanwhile, inverted staggered structures, which are the structures generally adopted in the fabrication of conventional a-Si:H TFTs, have been employed in most prototype displays. However, this