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Patterning of porous silicon nanostructures and eliminating microcracks on silicon nitride mask using metal assisted chemical etching

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ABSTRACT

A method for selective formation of reproducible, high fidelity and controllable nano and micrometer size porous Si areas over n-type Si wafers is provided. A 400 nm thick Silicon Nitride layer was used as the mask layer while Platinum and Palladium nanoparticles were deposited over the unprotected areas to obtain porous areas through metal assisted chemical etching process. Nanoparticles were deposited by electroless plating solutions containing H_2PtCl_6 and $PdCl_2$. Good controls over pore size and depth were obtained with well defined and sharp edges of the patterned areas. The results were compared to porous structures obtained via electrochemical etching process, indicating the superiority of metal assisted etching in terms of its simplicity as well as the ability of Silicon Nitride layer acting as the mask layer.

1. Introduction

Porous silicon was discovered by Uhlir in 1956 [1] and is characterized by high resistivity, large surface to volume ratio and high chemical activity [2]. In 1990, Canham reported bright, visible photoluminescence at room temperature from porous silicon (PS), produced by etching crystalline silicon (c-Si) electrochemically with hydrofluoric acid [3]. Based on these characteristics many applications have been proposed for PS such as optoelectronic devices [4,5], gas sensors [6–8] and humidity sensors [9]. The advantages of porous silicon as sacrificial layer for micromechanical microstructure as bridge and free standing cantilevers have been reported by Bell and his colleagues [10]. Recently, the use of porous Si in metal/porous Si schottky junctions has resulted into unprecedented applications in room temperature IR and gas detection [11]. It has also opened up the possibility of obtaining singe electron effect at room temperature easily [12,13].

Several methods have been used to form porous silicon such as stain etching [14], metal assisted etching [15–19]. Among these, electrochemical etching of silicon wafer in a solution that contains hydrofluoric acid, ethanol and DI water is the most common technique. Recently metal assisted etching has been proposed for porous formation in which nanoparticles deposited on the silicon surface provide holes necessary for chemical process that causes porosity. Nanoparticles such Pt, Pd, Ag and Au have been applied for this purpose [20,21].

Incorporation of porous silicon in integrated circuits requires the selective formation of porous areas and promising approaches for micron and submicron dimension have been reported. Using photoresists [22,23], ion irradiation or implantation masks [24], electron beam lithography [25], multilayer electrochemical resistant masks [26], Silicon carbide/silicon nitride masks [27] and Cr/Au mask [28] have been reported. A method for selective definition of the porous regions, must be compatible with today's integrated circuit fabrication techniques, not introduce impurities into the silicon substrate, not need to undesirable annealing steps, and not require exotic etching techniques to remove the masking layer. Such a technique should, preferably, be simple and allow good control of the pore size and depth. In this paper, for the very first time, a fabrication of porous structure using metal assisted etching with silicon nitride masks has been reported. It seems that this method can provide all the favorable characteristics mentioned above. The results have been compared to the case in which the porous samples were obtained by electrochemical etching.

2. Experimental details

In these experiments, 0.2 Ω.cm resistivity, (100) oriented n-type silicon wafers and 5–6 Ω.cm resistivity, (111) oriented n-type wafers with a 10 μm thick epi-layer of 5–6 Ω.cm resistivity, were used. The

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wafers were cut into 16 mm × 16 mm pieces and were cleaned with standard RCA procedure.

To act as an etch stop during silicon nitride etch, first a 700 Å silicon dioxide was deposited by dry oxidation at 1050 °C. Then, 400 nm Si_3N_4 was grown by low pressure chemical vapor deposition method. Over the silicon nitride layer a thermally evaporated Chrome was deposited to be used as the mask layer in the Si_3N_4 etching process. Cr layer was defined by Ceric Ammonium Nitride (NH_4NO_3.Ce $(NO_3)_3$) and silicon nitride was dry etched exposing four 0.25 mm^2 SiO_2 areas which were subsequently etched by HF.

Exposed Si areas were made porous either by photoelectrochemical etching or metal assisted etching. In photoelectrochemical etching, a Pt mesh was used as the counter electrode and a circular Cooper plate at the back side of the silicon wafer made an ohmic contact and acted as the anode electrode. The anodization solution was composed of 1 vol. HF (40 wt.%), 2 vol. ethanol and 1 vol. DI water, etching time was 15 min, and current density was kept at 30 $mA.cm^{-2}$. Samples were illuminated by 100 W tungsten lamp. After etching process the samples were rinsed in DI water and dried in the air.

In metal assisted etching, platinum and palladium nanoparticles were first deposited by electroless plating, using organometallic precursor solutions containing H_2PtCl_6 [29] and $PdCl_2$ [30], respectively. Samples were immersed in the deposition solution for 120–150 s and immediately transferred to be etched by 3 vol. fresh Hydrogen peroxide (30 wt.%) and 1 vol. HF acid(40 wt%). Such Pt coated samples were immersed inside the solution for 2 and 4 min and Pd samples for 5 min. The samples were then rinsed in DI water and dried in the air.

Note that, in metal assisted etching no electrical current and illumination is needed because the nanoparticles act as local cathodes to mediate the reduction of hydrogen peroxide and consequent hole injection necessary for chemical reactions that cause porosity.

All SEM images are taken by a HitachiI field emission scanning electron microscope operating at 15 KV. All atomic force microscope images are prepared by DME-SPM atomic force microscope scanning at AC mode equipped with a silicon tip working at tapping mode. The luminescence spectroscopy is performed by spectrophotometer. The light source is He-Cd laser emitted at 325 nm.

3. Results and discussions

3.1. Morphology of metal nanoparticles

Fig. 1 shows SEM images of the Si wafer covered with Pt and Pd nanoparticles for different immersion times in the electroless deposition solutions. The metal particles are different in diameter and vary between a few nanometers to several hundred nanometers for both of Pt and Pd particles. Fig. 1a shows silicon surface after 3 min immersion of sample in $PdCl_2$ solution. Fig. 1b shows Pt nanoparticles after 60 s of immersion time in Pt electroless plating solution. The adhesion of metal nanoparticles to silicon substrate for both of the Pt and Pd particles was weak; therefore, the samples had to be transferred into etching solution without being disturbed. It is clear that the density of nanoparticles increases with immersion time. In order to obtain more uniform deposition of nanoparticles on the sample surface, the solution was agitated at all time.

As etching starts, metal nanoparticles act as local cathode to mediate the reduction of H_2O_2 and cause the consequent hole injection necessary for etching reaction. A sufficient amount of holes (h^+) should be supplied by the oxidizing agent in order to maintain the etching at reasonably fast rate. Nanoparticles in the porous structure are shown in the following sections. The following relations describe chemical reactions occurring at cathode (metal) and anode (Si):

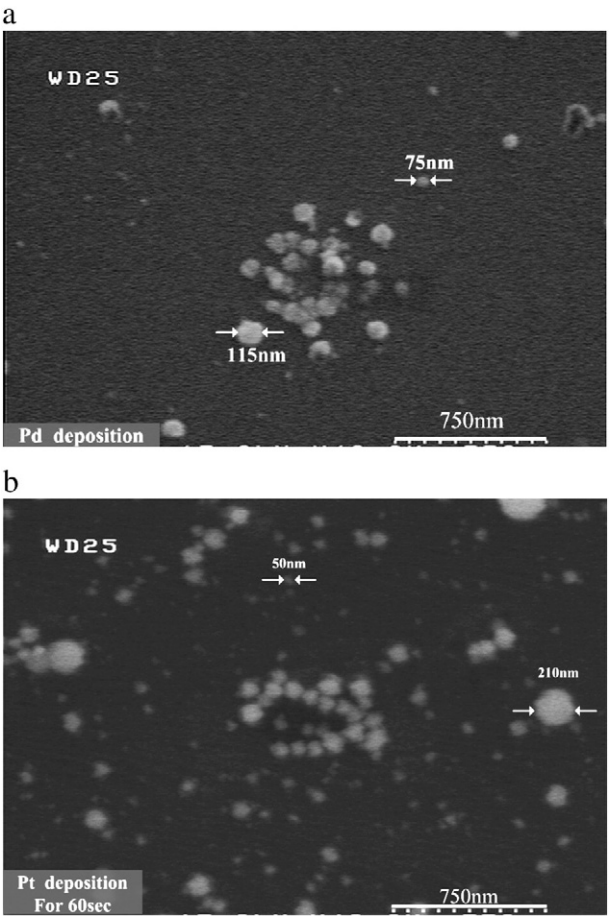

Fig. 1. SEM image of Si wafers after loading metal nanoparticles. (a) Pd nanoparticle deposition for 3 min (b) Pt nanoparticle deposition for 1 min.

Cathode (metal)

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \quad (1)$$

$$2H^+ \rightarrow H_2 + 2h^+ \quad (2)$$

Anode (Si)

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \quad (3)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (4)$$

Overall

$$Si + H_2O_2 + 6HF \rightarrow 2H_2O + H_2SiF_6 + H_2 \quad (5)$$

3.2. Resistance of Si_3N_4 mask in etching process

In our experiments the silicon nitride layer was exposed to chemical etching solution and microcracks were created in this layer during electrochemical etching process as it has been reported earlier in the literature [28]. Here in this research, the metal assisted chemical etching, however, does not cause any cracks and silicon