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# Effects of double passivation for optimize DC properties in gamma-gate AlGaN/GaN high electron mobility transistor by plasma enhanced chemical vapor deposition

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ABSTRACT

Two different materials for double passivation layers have been implemented to an AlGaN/GaN high electron mobility transistor on Si (111) substrate and the improved DC properties are demonstrated. $Si_3N_4$ and $SiO_2$ passivation materials are deposited on the gamma gate upper and bottom layers by plasma enhanced chemical vapor deposition. The gamma shape gate can be made by selectively accurate $Si_3N_4$ or $SiO_2$ first passivation dry etching with wet etching. The second passivation on gamma gate effectively increases the DC properties. The effects of DC properties of $Si_3N_4$ or $SiO_2$ single passivation and $Si_3N_4/Si_3N_4$ or $SiO_2/SiO_2$ double passivations are compared. The $Si_3N_4/Si_3N_4$ double passivation shows the maximum saturation current density and the peak extrinsic transconductance which increases up to 72% and 18%, respectively, more than $Si_3N_4$ single passivation and also up to 18% and 5% than $SiO_2/SiO_2$ double passivation.

## 1. Introduction

AlGaN/GaN based high electron mobility transistors (HEMTs) are now a key component in active devices, such as in high power amplifiers and various microwave and RF system applications [1]. The properties of AlGaN/GaN HEMTs are a high power handling capability, a wide band gap, a high breakdown voltage, a high current density, and a high saturation velocity. In addition, recent studies into the development of their fabrication techniques show that the quality of the GaN layer has been enhanced using sapphire ($Al_2O_3$), SiC, Si, diamond and specially grown GaN substrate [2–4]. In spite of their lattice and thermal expansion coefficient mismatches, high dislocation density and the possibility of crack, these hetero epitaxial growth structures nearly approach a homo epitaxial performance. However, one of the commonly significant issues that still remain in AlGaN/GaN HEMT is the current collapse problem due to the surface trap effect. Most AlGaN/GaN HEMTs also have a very shallow and sensitive two-dimensional electron gas channel. Without passivation, the exposed of the AlGaN/GaN epi-layer can be greatly affected and can be damaged by oxidation, moisture, and other forms of pollution. The application of various passivation materials, such as $SiO_2$ [5,6], $Si_3N_4$ [7–9], $SiO_xN_y$ [10], $Sc_2O_3$ [7,11], AlN [12], $HfO_2$ [13] and MgO [7,14] for passivation on the surface of the epi-layer is under researched. In addition, there are many different passivation methods and deposition techniques used to reduce current collapses and to improve the performance [15–19]. In this study, a double-insulator scheme is used in which $Si_3N_4/Si_3N_4$ or $SiO_2/SiO_2$ is deposited onto the top and bottom gamma gate surface passivation films layers on AlGaN/GaN HEMT by plasma enhanced chemical vapor deposition (PECVD). Silicon nitride and Silicon dioxide are the most widely popular passivation materials used to improve the performance of AlGaN/GaN HEMTs.

## 2. Experimental procedure

In this work, the Si (111)-based AlGaN/GaN HEMT fabrication process was used, which is highly competitive in terms of device performance and effective cost. The AlGaN/GaN epi-layers were grown by employing metal organic chemical vapor deposition on a 4-inch Si (111) substrate, composed of a 0.1 μm undoped AlN, a 1.2 μm GaN buffer layer, followed by a 50 nm undoped GaN layer, a 3 nm undoped $Al_{0.3}Ga_{0.7}N$ spacer, a $4.5\times10^{18}\,cm^{-3}$ Si-doped $Al_{0.3}Ga_{0.7}N$ layer and capped by a 5 nm undoped $Al_{0.3}Ga_{0.7}N$ layer. Fig. 1 shows the transmission electron microscopy (TEM) images of AlGaN/GaN epi-layers and Si (111) substrate with 0.1 μm undoped AlN. Through the selected area diffraction (SAD) image of Si (111) and 0.1 μm undoped AlN, the threading dislocation density of Si (111) substate and 0.1 μm undoped AlN is $2.73\times10^8\,cm^{-2}$ and $5.08\times10^8\,cm^{-2}$, respectively. The fabrication of the device was initiated using a conventional mesa-isolation method employing inductively coupled plasma (ICP) etching. The source and drain ohmic contacts, with a source-drain spacing $L_{sd}$ of 5 μm, were realized by the evaporation of Ti/Al/Ta/Au (20/80/40/100 nm) followed by rapid thermal annealing at 700, 750, 800, 850, and 900 °C for 2, 15, and 30 s under an $N_2$ atmosphere. The specific contact resistances (ρc) were recorded by transmission line model (TLM) measurements;

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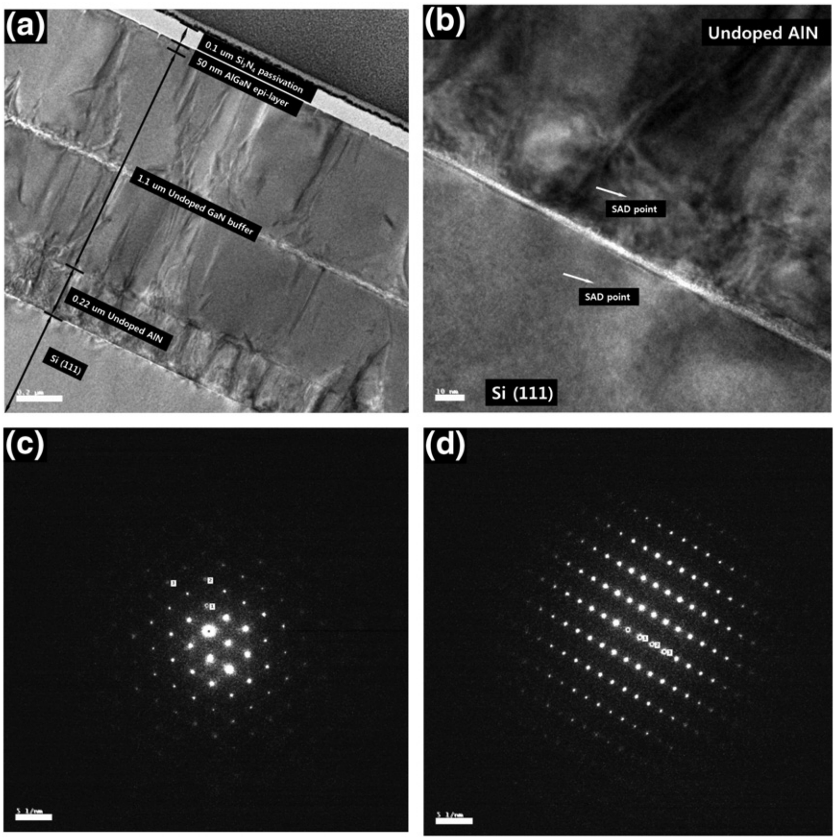

**Fig. 1.** TEM image of (a) cross-section of Si(111) substrate with epi-layers, (b) Si(111) substrate with undoped AlN layer, SAD image of (c) Si (111) and (d) undoped AlN.

the square (100 × 100 μm) contacts were separated by 2, 4, 8, 16 and 32 μm. The circular TLM data indicated a ρc of below $10^{-5}$ Ohm cm$^2$ with a sheet resistance of around 400 Ohm/sq.

In order to attach the bottom of the gate onto the undoped $Al_{0.3}Ga_{0.7}N$ (the top of the epi-layer), the $Si_3N_4$ or the $SiO_2$ is etched out using a dry/wet etching method to avoid free damage of the epitaxy materials. First, 80 nm of the $Si_3N_4$ or $SiO_2$ is dry-etched by an ICP etching system and then the remaining 20 nm of the $Si_3N_4$ or $SiO_2$ is wet-etched by a 1:6 buffer oxide etch (BOE) solution. Because the BOE is very sensitive to pattern size, film quality, and environment condition, a dummy wafer is needed during the overall dry/wet etching process. Subsequently, a Ni/Au (40/400 nm) gamma gate, with a length of 0.5 μm, was deposited at 0.5 μm shifted photo resistor gamma-gate pattering. Fig. 2 shows image of the cross sectional gamma gate process, which was conducted at a 0.5 μm gate pattering shift after the $Si_3N_4$ or $SiO_2$ dry etching and wet etching. After the deposition of the Ni/Au (40/400 nm) gate by an electronic-beam evaporator, $Si_3N_4$ or $SiO_2$ second dielectric layers were deposited on top of the gate. An analysis of the top and bottom gate passivation was conducted for the four cases shown in the focused-ion beam (FIB) images of Fig. 3: (A) 100 nm $Si_3N_4$ first passivation and 100 nm $Si_3N_4$ from the second gate passivation; (B) 100 nm $SiO_2$ from the first passivation and 100 nm $SiO_2$ from the second gate passivation; (C) 100 nm $Si_3N_4$ from the first passivation and without second passivation; (D) 100 nm $SiO_2$ from the first passivation and without second passivation. All of the experiments are referenced to the single passivation layer case. All $Si_3N_4$ and $SiO_2$ consist of 50% tensile and 50% compressive deposition stress. Chamber pressures of 111.4 and 151.9 Pa, chamber temperatures of 150 and 250 °C, RF frequency of 13.56 MHz and RF powers of 60 and 100 W were used for the respective $Si_3N_4$ and $SiO_2$ PECVD.

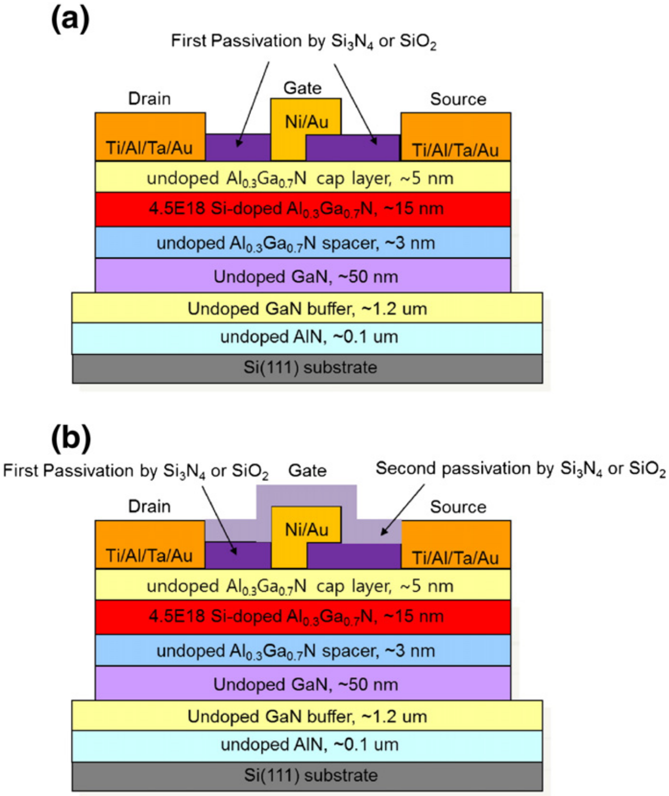

**Fig. 2.** Schematic representation of (a) single and (b) double passivation in AlGaN/GaN HEMT.