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Generation of uniaxial tensile strain of over 1% on a Ge substrate for short-channel strained Ge *n*-type Metal–Insulator–Semiconductor Field-Effect Transistors with SiGe stressors

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ABSTRACT

Tensile strain of over 1% in Ge stripes sandwiched between a pair of SiGe source-drain stressors was demonstrated. The Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET)-like structures were fabricated on a (001)-Ge substrate having SiO_2 dummy-gate stripes with widths down to 26 nm. Recess-regions adjacent to the dummy-gate stripes were formed by an anisotropic wet etching technique. A damage-free and well-controlled anisotropic wet etching process is developed in order to avoid plasma-induced damage during a conventional Reactive-ion Etching process. The SiGe stressors were epitaxially grown on the recesses to simulate strained Ge *n*-channel Metal–Insulator–Semiconductor Field-Effect Transistors (MISFETs) having high electron mobility. A micro-Raman spectroscopy measurement revealed tensile strain in the narrow Ge regions which became higher for narrower regions. Tensile strain of up to 1.2% was evaluated from the measurement under an assumption of uniaxial strain configuration. These results strongly suggest that higher electron mobility than the upper limit for a Si-MOSFET is obtainable in short-channel strained Ge-*n*MISFETs with the embedded SiGe stressors.

1. Introduction

Introduction of strain to channels has become a mature technology for high drive current by enhancing the carrier mobility in Si-Complementary Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) devices [1,2]. Concerning *n*MOSFETs, the electron mobility in strained Si channels, however, is limited to up to around twice that of unstrained Si channels [3]. It has been reported, on the other hand, that superior electron mobility (i.e. approximately 4 times higher than in unstrained Si channels and even higher than in tensile-strained Si channels), can theoretically be obtained in Ge channels by applying tensile strain of approximately 1% or higher to them [4]. Tensile strain can be generated by GeSn virtual substrates beneath the Ge channels or SiGe Source/Drain (S/D) stressors adjacent to the Ge channel region as shown in Fig. 1. The latter can be formed thanks to Selective Epitaxial Growth. We then end up with a configuration similar to that of Si:C S/D stressors, which have a smaller lattice parameter than that of Si and are used to generate for tensile-strained Si channels [2,5]. In addition, diode characteristics fabricated in strained SiGe layers on Ge substrates suggest advantages of SiGe S/D stressors such as better short-channel characteristics due to a smaller diffusion coefficient of P-dopants and lower Band-To-Band-Tunneling leakage currents due to the wider band gap of SiGe than that of Ge [6]. However, tensile strain in realistically scaled Ge Metal–Insulator–Semiconductor Field-Effect Transistor (MISFET) structures has not been observed, although the generation of large tensile strain in Ge substrates near dummy-gate edge regions adjacent to SiGe stressors has been experimentally observed with long-channel SiO_2 dummy-gated strained Ge structures [7]. In this paper, fabrication of the strained Ge structures having SiO_2 dummy gate scaled down to 26 nm, which is transparent for the laser beam used in Raman scattering measurement, and the application of strain to the ultra-scaled Ge channels are presented.

2. Experimental details

A Chemical Vapor Deposition (CVD)-grown SiO_2 dummy-gate layer was patterned into Line/Space stripes (L/S) (=26–130 nm/170–480 nm) parallel with a [011] direction on a HF-cleaned Ge(100) substrate. Subsequently, 0–100 nm-depth recess structures were anisotropically etched on the exposed Ge surfaces with the optimum $HCl + H_2O_2$ (HPM) solution following HF cleaning [7,8]. After the recess etching, the Ge surfaces were cleaned with HCl solution as pre-epitaxy cleaning. 10–110 nm embedded (i.e. 10 nm elevated from channel surfaces) SiGe stressor layers with the Ge composition, *x*, of 0.6, 0.7, 0.8, 0.9 and 1.0 were selectively grown on the recessed region in a hot-wall Low Pressure – CVD chamber using SiH_4 and GeH_4. The growth temperature and pressure were 450 °C and 1 Pa,

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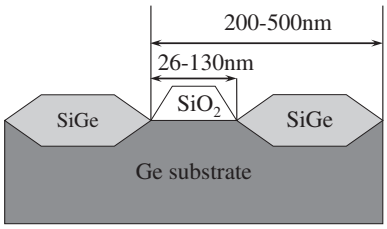

Fig. 1. A schematic cross-sectional view of the fabricated strained Ge structure with embedded SiGe stressors.

respectively. The Ge composition was determined with X-Ray Diffraction (XRD; Philips, X'Pert PRO MRD) measurements by using blanket SiGe films simultaneously grown in the same batch. Here, Ge composition and relaxation rates can be determined precisely thanks to coplanar XRD with asymmetric reflection using the protocol described in reference [9]. The sample structures were observed with Scanning Electron Microscope (SEM; Hitachi, S-4800, 10 kV operation) and Transmission Electron Microscope (TEM; Hitachi, H-9000NAR, 300 kV operation). Here, SiGe films grown on the patterned wafers were thicker than those on blanket wafers, probably due to loading effects. Those film thicknesses, therefore, were not determined with XRD but with SEM and/or TEM. The strain injected in the Ge layers was measured with micro-Raman spectroscopy (Jovin-Yvon, LabRAM HR); an Ar laser with wavelength of 488 nm was used as the light source, with a beam spot size of approximately 1 μm in diameter.

3. Results and discussion

Firstly, Ge recess regions for embedded SiGe stressors are formed by anisotropic wet etching. For this purpose, a damage-free and well-controlled anisotropic wet etching process is developed in order to avoid plasma-induced damage on Ge surfaces in a conventional Reactive-ion Etching process. Moreover, the wet etchant for Ge recess etching was optimized to minimize the undercut beneath the dummy-gate edges. This is necessary to control the alignment of the SiGe stressors against the gate stack and the sidewalls of the MISFETs. Thus, anisotropic wet etching, in which the etching rate of Ge(111) planes is the lowest, is suitable for minimizing the undercut region. In addition, HF-free wet etchant is strongly desired to prevent unintentional dummy-gate etching. To satisfy this condition, diluted HPM solution is selected and its concentration is optimized for high etching-rate ratio of Ge(100) planes to Ge(111) planes. For example, a SEM image of the 40 nm-depth etched region, which was defined by (111) and (100) planes, by the HPM solution is shown in Fig. 2. It is clearly shown, as a result, that the designed structures having faceted

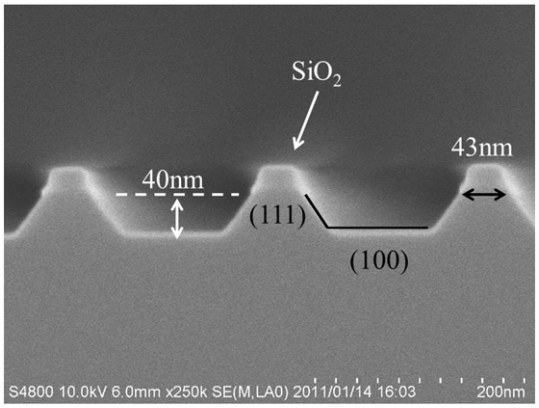

Fig. 2. A cross-sectional SEM image of Ge substrate recessed with HPM anisotropic etching.

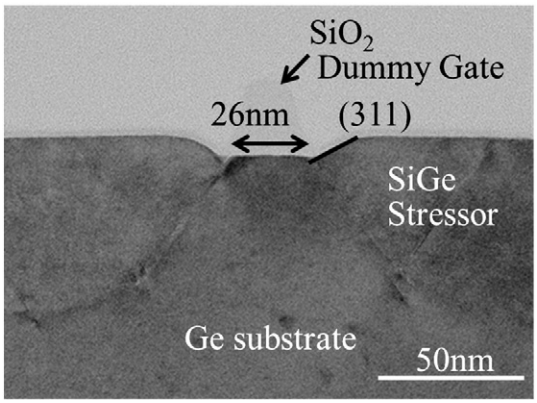

Fig. 3. A cross-sectional TEM image of 26 nm SiO_2 dummy-gated strained Ge structures with SiGe stressors with x of 0.7.

smooth surfaces are obtained with the HPM etching. Next, SiGe stressors were selectively grown on the Ge recess regions in the manner described in the reference [7]. It is confirmed that Ge-rich SiGe stressors having flat surfaces were grown in the recess regions whereas no nucleation was observed on the SiO_2 dummy gates even using a hot-wall reactor as shown in Fig. 3, although no etching gasses were employed. From this image, it is experimentally shown that; (i) Ge recess is formed with the HPM solution, (ii) epi-grown surfaces and recess interfaces are atomically flat, (iii) SiGe stressors are grown seamlessly with Ge channel region even under the dummy-gate edges, (iv) facets are formed on SiGe stressor surfaces near the dummy-gate edges, and (v) only a few stacking faults are observed in SiGe stressors. Here, it is considered that the facet formation around the elevated S/D edge is advantageous for reducing the gate-to-S/D capacitance of the MISFET compared to a seamless elevation to the sidewall. On the other hand, the formation of these stacking faults may induce some additional junction leakage. However, most of the strain due to the stressor is expected to remain. Indeed, defect densities close $1.0\times10^5\ cm^{-1}$ for $x=0.7$ and lower than $7.0\times10^3\ cm^{-1}$ for $x=0.8$, result in a slight strain relaxation only. Here, these defect densities were measured thanks to plan-view TEM. These experimental results indicate that anisotropic wet recess etching followed by selective epitaxial growth can be used to fabricate embedded SiGe stressors in Ge-*n*MISFETs. Next, let us discuss Raman measurements' results. Fig. 4 shows a plan-view SEM image of fabricated strained Ge channels having a 26 nm-long SiO_2 dummy-gate and SiGe stressors with Ge composition of 0.7. Here, 5–6 Ge channels are included in a Raman beam spot. In addition, average value of Line-Width-Fluctuation of SiO_2 dummy-gate

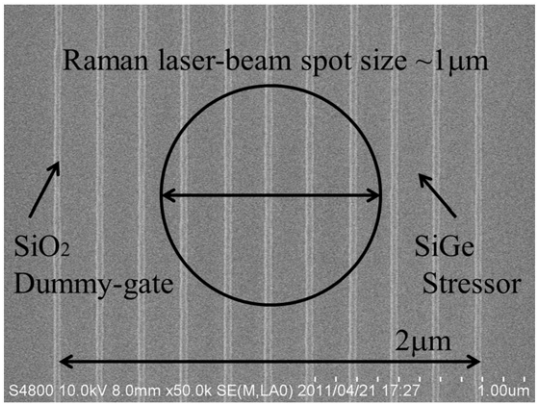

Fig. 4. A plan-view SEM image of SiO_2 dummy-gated strained Ge structures (L/S = 30/170 nm) with SiGe stressors with x of 0.7. Around 5 strained Ge channels are included in a Raman beam spot.