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Solid-phase epitaxy of undoped amorphous silicon by in-situ postannealing

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ABSTRACT

The solid phase epitaxy (SPE) of undoped amorphous Si (a-Si) deposited on SiO_2 patterned Si(001) wafers by reduced pressure chemical vapor deposition (RPCVD) using a H_2–Si_2H_6 gas system was investigated. The SPE was performed by applying in-situ postannealing directly after deposition process. By transmission electron microscopy (TEM) and scanning electron microscopy, we studied the lateral SPE (L-SPE) length on sidewall and mask for various postannealing times, temperatures and a-Si thicknesses. We observed an increase in L-SPE growth for longer postannealing times, temperatures and larger Si thicknesses on mask. TEM defect studies revealed that by SPE crystallized epi-Si exhibits a higher defect density on the mask than at the inside of the mask window. By introducing SiO_2-cap on the sample with 180 nm Si thickness following postannealing at 570 °C for 5 h, the crystallization of up to 450 nm epi-Si from a-Si is achieved. We demonstrated the possibility to use this technique for SiGe:C heterojunction bipolar transistor (HBT) base layer stack to crystallize Si-buffer layer to widen the monocrystalline region around the bipolar window and to improve base link resistivity of the HBT.

1. Introduction

The silicon–germanium (SiGe) heterojunction bipolar transistor (HBT) technology has undergone great developmental progress over the last decades. Many breakthroughs in areas of scaling and reduction of parasitics have led to today's advanced process concepts for HBTs with improved power and frequency capabilities as well as higher reliability [1]. The state of the art shows that high-speed SiGe:C HBT technology can be now constructed up to transit frequency/maximum oscillation frequency/breakdown voltage for common-emitter configuration values of 300 GHz/500 GHz/1.6 eV [2]. Due to the constantly growing needs for faster data communication rates and upcoming fields of application up to the terahertz region, innovative engineering solutions and techniques are required for further improvements in HBT design and device performance [2].

One possible approach to improve HBT device performance could be the reduction in base link resistivity. To achieve this, solid phase epitaxy (SPE) could be a suitable engineering method. This special technique of epitaxial crystal growth reorders under certain annealing conditions atoms of an amorphous layer structurally onto a crystalline template layer by layer [3,4]. Until now, SPE was already used for reshaping the crystal structure in Si-on-insulator, thin-film transistor and liquid crystal display technologies [5–8]. However, almost no study of using SPE for bipolar transistor structures has been reported yet. Therefore, we focused recently on using the SPE technique for possible emitter application in HBTs by reporting SPE results of As-doped a-Si on SiO_2/Si_3N_4 patterned Si(001) wafers using reduced pressure chemical vapor deposition (RPCVD) with an H_2–Si_2H_6–AsH_3 gas system for deposition and in-situ postannealing [9].

In this work in order to evaluate the possibilities of using the SPE technique in an HBT base test process, we studied the lateral SPE (L-SPE) growth behavior of a-Si deposited differentially on SiO_2 patterned Si(001) wafers by RPCVD using a H_2–Si_2H_6 gas mixture.

2. Experimental details

Both deposition process of a-Si/epitaxial Si (epi-Si) and SPE of deposited a-Si on SiO_2-mask were carried out by using a lamp-heated single wafer RPCVD system. For the sample preparation, Si(001) wafers with an 80 nm thick SiO_2-mask on top and a model bipolar window structure for the current HBT technology of IHP with overhanging sidewall [2] were used. Then, selective Si (sel. epi-Si) is deposited into bipolar window at 800 °C by RPCVD using a H_2–H_2SiCl_2–HCl gas mixture to planarize the surface of the wafer. For experiments, the prepared patterned Si wafers were chemically cleaned in a standard RCA solution combined with HF last clean. Afterwards, the Si wafers were loaded in the reactor and baked at 850 °C in H_2 to form oxygen free Si-surface. Subsequently, up to 180 nm Si was deposited differentially at 550 °C using H_2–Si_2H_6 gas mixture, creating epi-Si and a-Si on Si and SiO_2 mask, correspondently (Fig. 1(a)). To investigate the influence of surface migration effects on SPE, a-Si/epi-Si surface of some samples were fixed

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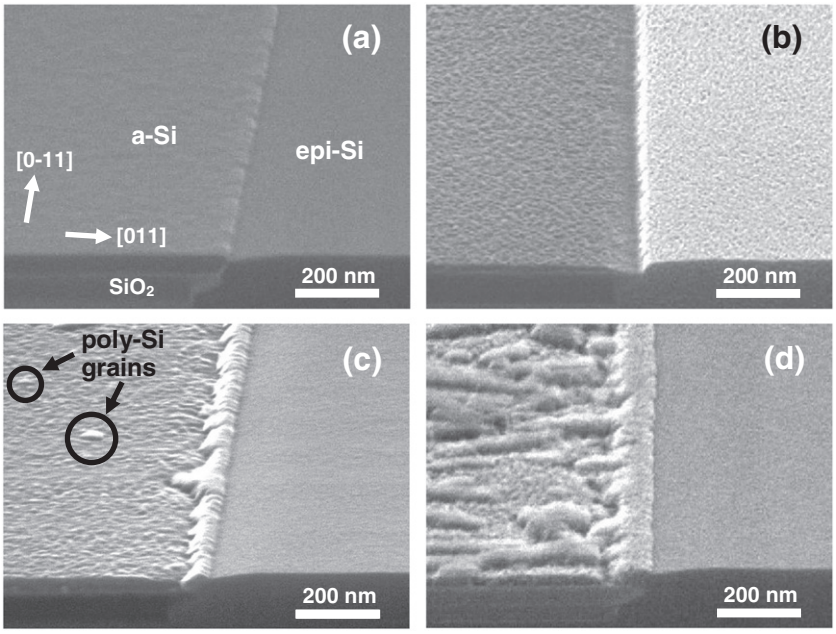

Fig. 1. Angle view (10°) of SEM pictures of as-deposited (a), with following Godbey etching (b), as well as postannealed at 550 °C (2 h and 5 h) and Godbey etched samples (c)–(d). Si thickness on mask is 50 nm. Godbey etching of a-Si was performed at room temperature.

by capping with 10 nm PECVD SiO_2 deposited at 400 °C as an optional intermediate process step. Directly after that, the SPE of deposited undoped a-Si was induced by postannealing the samples in-situ in the RPCVD chamber varying postannealing times and temperatures as well as the deposited a-Si thickness on mask for investigation. During postannealing process the reactor was always kept under steady H_2-flow and at reduced pressure.

Cross section transmission electron microscopy (TEM) and scanning electron microscopy (SEM) were used to evaluate the crystallinity and the mean L-SPE crystallization length. All TEM lamellas were prepared by mechanical grinding and polishing combined with an ion milling process. The following TEM measurements were carried out by a Philips CM 200 transmission electron microscope operating at 200 kV. For scanning electron microscopy (SEM) analysis, a Hitachi S-4500 scanning electron microscope operating with an acceleration voltage of 25 kV was used. The L-SPE domain length was determined using TEM/SEM starting from the edge of the epitaxially crystallized a-Si part until transition to a-Si or poly-Si domain on the mask. Because the crystallization front on SiO_2 mask is not straight and parallel to the sidewall, we determined an average L-SPE length by angle view SEM images. The observed fluctuation between maximum and minimum extension of L-SPE length is expressed in the form of error bars in the following figures. For the SEM analysis, selective etching of a-Si and poly-Si based on Godbey solution was performed to emphasize the crystallized epi-Si domain and poly-Si grains (Fig. 1(b)–(d)) [9–11].

3. Results and discussion

Before introducing SPE process, a selective etching on as-deposited samples was performed indicating no crystallization of a-Si at the sidewall or formation of poly-Si grain seeds on the mask during deposition process (Fig. 1(b)). By applying in-situ postannealing at 550 °C in the RPCVD chamber, a-Si was crystallized laterally near the sidewall of the mask window (Fig. 1(c)). On SiO_2 mask few scattered poly-Si grains could be observed originating from random crystallization of their grown nuclei seeds. With increasing postannealing time, crystallized Si domain near the sidewall grew up. Additionally, poly-Si grain formation and poly-Si grain size becomes larger on the mask (Fig. 1(d)).

To determine both crystallinity of crystallized epi-Si domain and their dependence on various postannealing temperatures, cross section TEM images after 550 °C and 570 °C for 2 h are shown in Fig. 2, respectively. We chose this postannealing temperature region due to preliminary experimental results with higher postannealing temperatures, which showed an undesirable increase in surface roughness and an SPE obstructing full formation of poly-Si on the mask. Fig. 2(a) revealed that before the SEM observed crystallized Si domain

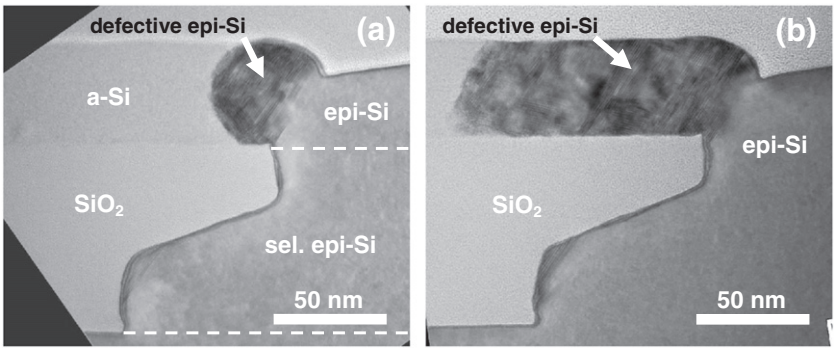

Fig. 2. Cross section TEM images of samples postannealed at 550 °C (a) and at 570 °C (b) for 2 h. Si thickness on mask is 50 nm.