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Improvement of Al_2O_3/Ge interfacial properties by O_2-annealing

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ABSTRACT

The electrical properties of an Al_2O_3/Ge gate stack structure were improved by O_2-annealing. The interface state density can be decreased by O_2-annealing without the formation of a GeO_2 interfacial layer. X-ray photoelectron spectroscopy measurements revealed that Ge diffusion into the Al_2O_3 layer occurs and Ge is uniformly distributed in the oxide layer after O_2-annealing. Crystallization of the Al_2O_3 film was observed after O_2-annealing at 550 °C and was identified as an Al–Ge–O compound using cross sectional transmission electron microscopy and transmission electron diffraction measurement.

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1. Introduction

To realize ultra-high speed Ge channel metal-oxide-semiconductor field-effect transistors (MOSFETs), high dielectric constant film (high-k)/Ge gate stack structures with both low interface state density ($<10^{11}$ $eV^{-1}\cdot cm^{-2}$) and low equivalent oxide thickness (<1 nm) must be developed. The high interface state density (10^{12}–10^{13} $eV^{-1}\cdot cm^{-2}$) and Ge diffusion into the high-k are caused by the direct junction of high-k and Ge [1–3]. Interface states are one of the causes of remote coulomb scattering, which causes degradation of the effective carrier mobility [4]. Therefore, control of the high-k/Ge interface is very important to realize a low interface state density. In addition, Ge diffusion into the high-k causes a decrease in the dielectric constant of the high-k [5,6]. Therefore, we have focused on the introduction of an interfacial layer which realizes high thermal stability, a comparably high dielectric constant, and a low interface state density by control of the interfacial properties. Al_2O_3 has higher thermal stability and a higher dielectric constant than GeO_2[7]; however, the Al_2O_3/Ge structure generally has a higher interface state density than the GeO_2/Ge structure, which exhibits a low interface state density [8–12]. Therefore, with respect to MOSFET fabrication, the introduction of a thermally stable interfacial control layer is strongly required. It is therefore necessary to decrease the interface state density of the Al_2O_3/Ge structure if Al_2O_3 is to be used as an interfacial control layer. Zhang et al. reported that the formation of a GeO_2 interfacial layer by post plasma oxidation of the Al_2O_3/Ge structure is effective to reduce the interface state density [13]. The low temperature plasma process effectively introduces O only into the Al_2O_3/Ge interface, although there is a concern that plasma damage occurs by light exposure [14]. In contrast, an annealing process could be employed to introduce O into the Al_2O_3/Ge interface and also induce interfacial chemical reaction, without damage to the structure. In this study, we investigated the effects of annealing in N_2 and O_2 atmospheres on the electrical properties, interfacial structure, and chemical bonding states of the Al_2O_3/Ge gate stack structure.

2. Experiment

In-doped p-type Ge(001) wafers with a resistivity of 0.95–3.0 Ω-cm were used as substrates. After treatment with diluted HF to remove the native oxide on the substrate surface, a 1 nm thick Al_2O_3 layer (1st-Al_2O_3 layer) was deposited by the atomic layer deposition (ALD) method using a SUNALE™ R-150B reactor (Picosun) at a substrate temperature of 300 °C. For deposition of the Al_2O_3, trimethylaluminum (TMA) was used as a metal–organic precursor and H_2O as an oxidant. 200 sccm of pure N_2 gas was used as a carrier gas. The pulsing times of TMA and H_2O were 0.1 and 1.0 s, respectively. The N_2 purging time was 4.0 s and 10 ALD cycles were used. After deposition of the 1st-Al_2O_3 layer, the sample was annealed in N_2 or O_2 atmospheres for 30 s at temperatures ranging from 400 to 600 °C. N_2 and O_2 flow rates were both set at 1.5 L/min. AFM observation revealed that the surface morphology hardly changes with the 1st-Al_2O_3 deposition compared with that of the Ge substrate after chemical cleaning. Also, we cannot find the significant surface roughing in the sample after O_2-annealing. To fabricate a MOS capacitor, a 3 nm thick Al_2O_3 layer (2nd-Al_2O_3 layer) was deposited at a substrate temperature of 300 °C by the ALD method. Finally, the Al gate and Al backside electrodes were fabricated by vacuum evaporation.

Capacitance–voltage (C–V) measurements were used to investigate the electrical properties. The interfacial structure was examined by cross-sectional transmission electron microscopy (TEM) and the

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transmission electron diffraction (TED) using a JEM2010F (JEOL). The operating voltage was 200 kV. The sample for the TEM observation was prepared by the Ar ion milling. X-ray photoelectron spectroscopy (XPS) with Ar ion sputtering using an ESCA LAB210 (VG Scientific) was conducted to analyze the chemical bonding states. AlKα ($h\nu = 1486.6$ eV) line with an electrical power of 300 W was used as an X-ray source, and a take-off-angle was 90°. Energy of Ar ion used in sputtering was 3.0 keV and a pressure was 2×10^{-7} Torr. XPS measurement and Ar ion sputtering were alternately carried out in situ. The Ge substrate was connected to ground.

3. Results and discussion

Fig. 1(a)–(c) shows C–V characteristics of the Al/Al_2O_3/Ge capacitor (a) without annealing and (b) with N_2-annealing at temperatures of 400 and 550 °C, and (c) with O_2-annealing at temperatures of 400, 550, and 600 °C. The oxide capacitance decreases after N_2- and O_2-annealing at all temperatures. In particular, the oxide capacitance is significantly decreased after O_2-annealing at 600 °C. It is considered that the insulator film thickness is slightly increased after N_2- and O_2-annealing in the temperature of 400 and 550 °C, and this increase is most severe after O_2-annealing at 600 °C. A hump in the C–V characteristics is evident for the sample that was not annealed, which indicates the existence of the interface state. While the height of the hump does not decrease after N_2-annealing, it does decrease after O_2-annealing. In addition, the shift of the flat-band voltage from the ideal value decreases only after O_2-annealing. Therefore, the net negative charge of the Al_2O_3 film decreases.

Fig. 2 shows the interface state density as a function of the annealing temperature for the non-annealed sample and those samples annealed in N_2 and O_2. The high-low-frequency capacitance method was used to evaluate the interface state density. In this method, the capacitance related to the interface state density (C_{it}) and the interface state density (D_{it}) are expressed as follows:

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{max,LF}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{max,HF}}\right)^{-1}, \quad (1)$$

$$D_{it} = \frac{C_{it}}{q}, \quad (2)$$

where C_{LF} and C_{HF} are capacitances obtained by low (100 kHz) and high (1 MHz) frequency measurements, respectively, and $C_{max,LF}$ and $C_{max,HF}$ are the oxide capacitances obtained by low and high frequency measurements, respectively. After O_2-annealing below 450 °C, the interface state density decreases with the annealing temperature and shows a constant value as low as 1×10^{12} $eV^{-1}\cdot cm^{-2}$ after annealing at higher than 450 °C. In contrast, the interface state density increases with N_2-annealing temperatures higher than 450 °C. These results indicate that annealing in O_2 is a key factor to decrease the interface state density.

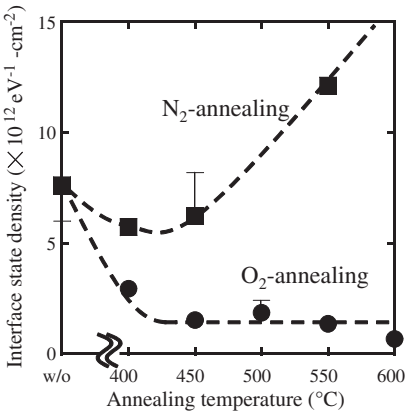

Fig. 2. Interface state density as a function of the annealing temperature.

Fig. 3(a)–(d) shows cross sectional TEM images of the 2nd-Al_2O_3/1st-Al_2O_3/Ge structures without annealing, after N_2-annealing at 550 °C, and after O_2-annealing at 400 and 550 °C, respectively. The thickness of the Al_2O_3 film in the non-annealed sample was evaluated as 4.0 nm and the Al_2O_3 film had an amorphous structure. Neither the thickness nor the crystalline structure of the Al_2O_3 film changed, even after N_2-annealing at 550 °C, as shown in Fig. 3(b). However, the thickness of the Al_2O_3 film was increased by 0.2 nm after O_2-annealing at 400 °C. Moreover, after O_2-annealing at 550 °C, a 0.7 nm increase of the Al_2O_3 film thickness and crystallization of the 1st-Al_2O_3 layer were observed.

Fig. 4(a) and (b)shows TED patterns of the non-annealed sample and the sample annealed in O_2 at 550 °C, respectively. Only diffraction spots related to a bulk-Ge substrate are evident in Fig. 4(a). However, in Fig. 4(b), parts of the diffraction rings are observed in addition to diffraction spots of bulk-Ge. The lattice spacings of these two diffraction rings were evaluated using some TED patterns of this sample, and were 0.16–0.18 and 0.27–0.29 nm. However, these lattice spacing do not correspond to the reported values for various crystalline structures of Al_2O_3 and GeO_2 [15]. XPS results reveal that an Al–Ge–O compound is formed after O_2-annealing at 550°C as discussed later. The diffraction rings shown in Fig. 4(b) probably indicate the presence of Al–Ge–O compounds in the insulator film. In addition, the parts of the diffraction rings are observed only along the Ge<001>direction, which indicates that this crystallized layer is weakly oriented.

Fig. 5(a)–(f) shows Al2p and Ge3d XPS spectra after Ar ion sputtering of the 1st-Al_2O_3/Ge samples without annealing, and those with N_2- and O_2-annealing at 550 °C, respectively. The intensities of all spectra were normalized according to the area intensity of the

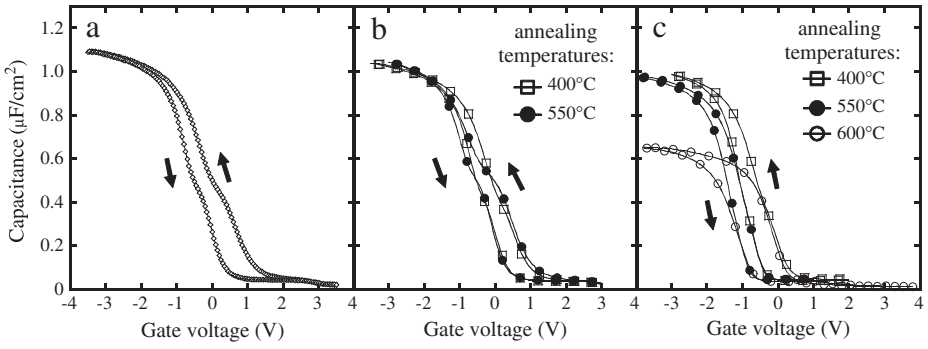

Fig. 1. Room temperature C–V characteristics (27 °C) of Al/Al_2O_3/Ge MOS capacitors (a) without annealing, (b) with N_2-annealing in the temperature of 400 and 550 °C and (c) with O_2-annealing in the temperature of 400, 550, and 600 °C.

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