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Damp heat stability of Al-doped zinc oxide films on smooth and rough substrates

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ABSTRACT

Properly encapsulated chalcopyrite-based solar modules from a number of manufacturers have passed the accelerated ageing tests in damp heat.
Non-encapsulated modules after damp heat exposure show an increased series resistance which is contributed significantly from the increase in lateral sheet resistance of the transparent Al-doped zinc oxide (ZAO) front contact. We have shown previously, that a rough substrate morphology (on a μm-scale) is a major influence in the ZAO degradation mechanism, due to local perturbations of the ZAO growth (*extended grain boundaries*).
To further model and examine the extended grain boundaries we present a study of the electrical properties of RF-sputtered ZAO films before and after damp heat, grown on rough quartz glass as well as on polished, texture-etched and patterned silicon. The pattern consisted of equidistant trenches and have a periodical two-dimensional geometry.
The strongest decrease of ZAO conductivity occurs on the patterned silicon substrate perpendicular to the trenches. The conductivity parallel to the trenches, however, had the same trend as the conductivity of ZAO on smooth silicon. Measured activation energies of the conductivity of 40 meV or less after damp heat are not sufficient to explain the drastic decrease of conductivity in terms of a grain-boundary-barrier theory (as described, e.g., by SETO). We will summarise our current understanding of the extended grain boundaries and present a refined barrier model to explain our experimental observations.

1. Introduction

Heavily doped zinc oxide films with a wide bandgap of 3.4eV are used as transparent and conductive electrodes in thin-film solar cells [1]. Properly encapsulated chalcopyrite-based solar modules from a number of manufacturers are certified according to *IEC/EN 61646* and have passed the accelerated ageing tests in damp heat (DH) which form a part of the specification [2–6]. Nevertheless, there is sufficient motivation to clarify the damp heat degradation observed without encapsulation. An inherently stable module could lower encapsulation costs and enable flexible products without glass/glass lamination. The increase in lateral sheet resistance of the transparent Al-doped zinc oxide (ZAO) front contact is known to contribute significantly to an increased series resistance and, consequently, lower fill factor of the non-encapsulated module after damp heat exposure.

We have shown previously [7], that a rough substrate morphology (on a μm-scale) is a major influence in the ZAO degradation mechanism, due to so called *extended grain boundaries* (eGB), which are local perturbations in the ZAO growth and consist of smaller grains with non orientated c-axis and a higher area fraction of grain boundaries.

To further model and examine the extended grain boundaries we present here a study of the electrical properties of ZAO films before and after damp heat, grown on a range of substrates: rough quartz glass and polished, texture-etched and patterned silicon. The pattern consisted of equidistant trenches prepared by photo-lithography. Temperature dependent conductivity- and Hall-measurements were carried out to characterise charge carrier concentrations and mobilities as well as activation energies before and after the damp heat ageing. We summarise our current understanding of the extended grain boundaries and present a refined barrier model to explain our experimental observations.

2. Experimental details

To simulate the rough, polycrystalline chalcopyrite absorber and buffer layer stack, various substrates of polished silicon, texture-edged silicon [3,8], bead-blasted quartz glass [7] and photo-lithographed silicon (Fig. 1) were prepared. The latter substrate has a patterned structure of equidistant trenches, which have the same depth of 1.5μm, but were, on different samples, spaced 1.5, 3 and 6μm apart ("structural width").The crest-to-trough-width-ratio was 1:1 for all structural widths. In contrast to the random roughness of the texture-edged and bead-blasted quartz glass, the patterned silicon substrates have a well defined two-dimensional geometry.

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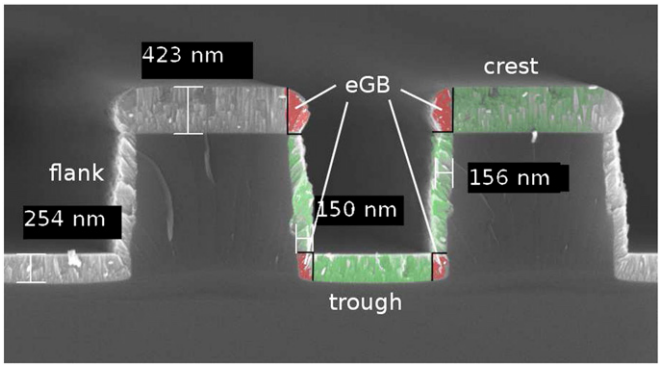

Fig. 1. Scanning electron micrograph (cross section) of ZAO on the patterned silicon substrate with 1.5μm structural width. One patterned period is coloured: The regions of compact ZAO growth on a locally smooth crest, trough and flanks are marked green and the regions of the eGB are marked red.

Highly Al-doped ZnO (ZAO) of about 400nm thickness was deposited by RF-sputtering from a ceramic $ZnO/Al_2O_3$1wt.% target. The substrates were fixed with respect to the magnetron (static deposition) and not intentionally heated. Samples were stressed in 85% relative humidity at 85°C. The total stress period of up to 1000h was repeatedly interrupted when the samples where removed from the DH chamber to be characterised under ambient conditions.

Cross-sectional ZAO on patterned silicon specimens for transmission electron microscopy (TEM) were prepared and investigated by high-resolution TEM. The roughness of the substrates was measured with a Dektak 8 profiler. The thickness of the ZAO layers was obtained by scanning electron microscopy and by fitting of optical transmission/reflection spectra (see [7]).

Temperature dependent Hall effect and conductivity measurements were done within a super-conductive helium bath cryostat with magnetic fields up to 6T in order to determine the conductivity σ, charge carrier concentration n and electron mobility μ. Those measurements were done in Van-der-Pauw geometry with evaporated Ni/Al contacts in the corners on the ZAO layer for the random rough samples. The patterned samples, however, were prepared only for conductivity measurements with independent current source and voltage measurement (four-contact configuration), schematically shown in Fig. 2. In this set-up the current injection is through the two outer contact stripes and, thus, the direction of the current density $\boldsymbol{j}$ is predetermined and well-defined. We define the parallel set-up, $\boldsymbol{j}||\boldsymbol{P}$, when the current flows parallel to the trenches (indicated by the patterning vector $\boldsymbol{P}$). In the perpendicular case, $\boldsymbol{j}\perp\boldsymbol{P}$, the current has to flow through the crest, trough and flanks.

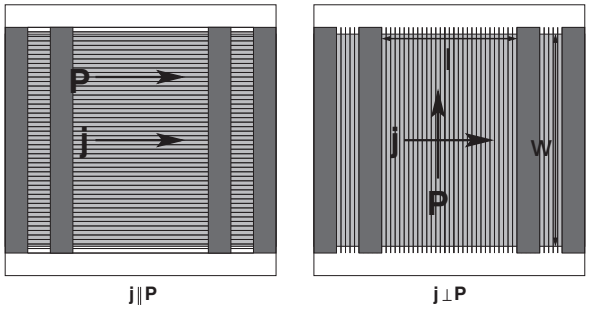

Fig. 2. Sample preparation: ZAO (grey) was sputtered on the patterned silicon substrate (black-white). The two outer Ni/Al contact stripes (dark grey) were used for the current injection and they define the direction of the current density $\boldsymbol{j}$ parallel (left) and perpendicular (right) to the patterning vector $\boldsymbol{P}$. The two inner contact stripes were used for the measurement of the voltage dropping over the distance l.

3. Results

The scanning electron micrograph (Fig. 1) shows a cross section of the ZAO on the patterned silicon. The ZAO grains are compact on the crest, trough and flanks of the trench but the ZAO grains grew irregularly on the corner of each trench and form an eGB. The average roughness $\mathcal{R}_a$ of typical absorbers and the substrates are given in Table 1. Note, due to the periodicity, the patterned silicon does not have a random roughness. In scanning electron and transmission electron micrographs of ZAO layers on the patterned silicon there was no structural difference before and after DH exposure visible.

The conductivity was evaluated under the assumption of a homogeneous, coplanar ZAO layer:

$$\sigma = \frac{1}{d_{eff}\langle R_{\square}\rangle}, \tag{1}$$

where d_{eff} is the effective layer thickness and $\langle R_{\square}\rangle$ is the average sheet resistance. For the patterned substrates the ZAO thickness on the crest was used as effective thickness and the periodicity was not taken into account yet (see Section 4). The conductivity at room temperature (Fig. 3) depends significantly on the roughness of the substrate, both before and after exposure to DH. This results in the following degradation ranking: polished silicon (most stable), patterned $\boldsymbol{j}||\boldsymbol{P}$ silicon, texture-edged silicon, bead-blasted quartz glass, patterned $\boldsymbol{j}\perp\boldsymbol{P}$ silicon with 6μm, 3μm and 1.5μmstructural width (most unstable). The ZAO conductivity on the patterned silicon in the $\boldsymbol{j}||\boldsymbol{P}$ set-up hardly differs from the conductivity on the polished silicon wafer. However, the difference in conductivity between $\boldsymbol{j}\perp\boldsymbol{P}$ and $\boldsymbol{j}||\boldsymbol{P}$ is bigger [9] than between the random rough and polished substrates.

The measurement of the Hall voltage of DH degraded ZAO layers on rough quartz glass with low conductivity is difficult even with magnet fields up to 6T. Nevertheless, temperature-dependent Hall effect and conductivity measurements of ZAO on polished, bead-blasted and texture-edged substrates between $45-300$K show almost no temperature dependence of the conductivity, charge carrier concentration and mobility. After the DH treatment, the charge carrier concentration is $\sim 10^{20}\mathrm{cm}^{-3}$. In addition, if one takes the high optical charge carrier concentration into account, which was determined from the plasma frequency (see [7]), we conclude that even the degraded ZAO layer remains a degenerate semiconductor. The decrease in conductivity is mainly caused by the decrease of mobility.

The most strongly degraded ZAO films on the $\boldsymbol{j}\perp\boldsymbol{P}$ patterned silicon show, however, a higher temperature dependence (Fig. 4). Although the ZAO is degenerated there is a small thermal activation of the conductivity.

4. Discussion

The comparison of the degradation of the conductivity under DH (Fig. 3) and the roughness of the random rough substrates (Table 1) shows a systematic correlation: rougher substrate morphologies lead to a stronger degradation of the ZAO conductivity. In particular the decrease of the conductivity on the patterned silicon is extremely

Table 1
Average roughness $\mathcal{R}_a$ of chalcopyrite absorbers and the substrates used in this work.

substrate	$\mathcal{R}_a$(nm)
$Cu(In, Ga)S_2$	255
$Cu(In, Ga)Se_2$	130
bead-blasted quartz glass	2420
polished silicon	<1
texture-edged silicon	525
photo-lithographed silicon	*750*