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# Spin injection, transport, and read/write operation in spin-based MOSFET

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ABSTRACT

We proposed a novel spin-based MOSFET "Spin-Transfer-torque-Switching MOSFET (*STS*-MOSFET)" that offers non-volatile memory and transistor functions with complementary metal-oxide-semiconductor (CMOS) compatibility, high endurance and fast write time using *STS*. The *STS*-MOSFETs with Heusler alloy ($Co_2Fe_1Al_{0.5}Si_{0.5}$) were prepared and reconfigurability of a novel spintronics-based MOSFET, *STS*-MOSFET, was successfully realized for the transport properties owing to reduction of the contact resistance in ferromagnetic metal/thin insulator tunnel barrier/Si junctions. The device showed magnetocurrent (*MC*) and write characteristics with the endurance of over $10^5$ cycles. It was also clarified that the read characteristic can be improved in terms of MC ratio, however, is deteriorated in terms of the mobility by choosing connection configurations of the source and the drain in the *STS*-MOSFETs.



## 1. Introduction

The shrinking of silicon (Si)-based conventional complementary metal–oxide–semiconductor (CMOS) transistors will reach its intrinsic physical limits in the future [1]. Since there is a scaling limit of CMOS, new devices capable of adding novel functions to Si-based CMOS transistors should be developed as beyond CMOS devices. Spintronics has attracted much attention as promising candidate to overcome this scaling limit. Spintronics enables remarkable improvement in device performance in terms of nonvolatility, reconstructibility, low power consumption, etc. In particular, group-IV semiconductor spintronics, compatible with existing Si-based semiconductor technologies, is strongly desired. Fortunately, Si is predicted to be a semiconductor with enhanced spin lifetime and spin transport length due to low spin-orbit scattering and lattice inversion symmetry. Using these characteristics, spin-dependent transport through Si channels has been observed by many researchers [2–11]. However, several issues need to be resolved in order to develop spin metal–oxide–semiconductor field effect transistors (MOSFET), proposed by Sugahara and Tanaka [12], such as (1) the lack of good spin manipulation and control method for Si-based spin MOSFET, because the way of spin manipulation proposed by Datta and Das [13] cannot be utilized owing to the small spin-orbit interaction for Si, (2) difficulties of spin injection and detection in the case of a semiconductor such as Si, and (3) preparation of high spin polarized ferromagnet (FM) on Si. In particular, high spin polarization from FM via tunnel barrier should be generated to enhance output signal. In half-metallic ferromagnet, Heusler alloy/MgO would be a promising candidate, because relatively high tunneling spin polarization has already been demonstrated in the cases of granular system and MTJs [14,15].

In terms of issue (1), we have proposed a novel spin-based MOSFET "Spin-Transfer-torque-Switching MOSFET (*STS*-MOSFET)" (Fig. 1) [7,16] that offers non-volatile memory and transistor functions with CMOS compatibility, high endurance and fast write time using spin-transfer-torque-switching (*STS*). Since this structure has magnetic multilayers such as magnetic tunnel junctions (MTJs) on the source or/and drain via tunnel barriers, we can utilize *STS* for the spin manipulation (write process). The critical current for the *STS* is proportional to the area of MTJ [17,18]. Therefore small MTJ contributes to the manipulation of spin directions. Moreover, we can utilize the double output signal originating from spin-dependent transport through Si and tunnel magnetoresistance (*MR*) from MTJs, when MTJs are used as the magnetic multilayers. The spin MOSFET directly couples the logic element with the nonvolatile memory element, opening up a path to a new kind of logic-in-memory architecture [19]. The most promising application for the spin MOSFET such as *STS*-MOSFET is a reconfigurable logic chip, which can reconfigure the logic data and can be applied to various logic products. Field Programmable Gate Array (FPGA) has a great advantage because a chip is completely programmable and reconfigurable. We have proposed new circuits for the FPGA using *STS*-MOSFET [20]. The area and speed of million-gate spin FPGAs are numerically benchmarked with CMOS FPGA for 22, 32, and 45 nm technologies including a 20% transistor size variation. We have showed that the area is reduced and the speed is increased in spin FPGA owing to the nonvolatile memory function of spin MOSFET [20]. In order to realize the spin FPGA, functions of *STS*-MOSFET should include non-volatile memory and transistor functions with CMOS

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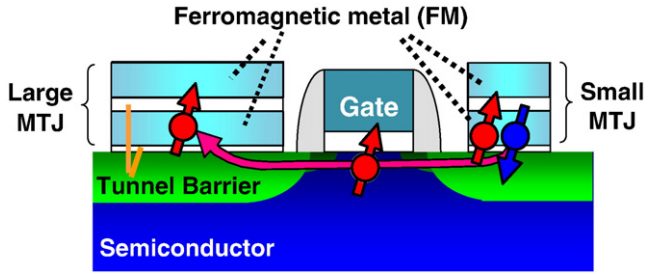


**Fig. 1.** Spin-based MOSFET of the "spin-transfer-torque-switching MOSFET (*STS*-MOSFET)" type in which magnetic tunnel junctions are attached to source and drain electrodes.

compatibility such as large on/off ratio of current flow, high endurance and fast write time. The large on/off ratio of current flow of *STS*-MOSFET can utilize when using p/n junction in Si and controlling a gate voltage as shown in Fig. 1.

In these contexts, new innovative ferromagnetic source/drain technologies for next-generation-transistor applications are researched and developed.

In this paper, first, we demonstrate low interface resistance of Si/tunnel barrier (I)/ferromagnet (FM) and high spin-polarization of FM. Next, utilizing the Si/MgO/Heusler alloy $Co_2Fe(Al_{0.5}Si_{0.5})$ (CFAS) interface, we show some data for electrical spin injection and detection in a Si-based device structure. Lastly, we demonstrate read/write operation and the endurance of *STS*-MOSFET and also present the detailed read and write characteristics of the *STS*-MOSFET.

We expect these novel results to lead to technology that opens path for development of next-generation spin transistors.

## 2. Device fabrication and experiments

The spin injection devices and back-gate *STS*-MOSFETs with MTJs were fabricated on Si (001) and p-type Si-on-Insulator (SOI) substrates. We used a heavily doped n-type Si surface (n+-Si) under the tunnel barrier (*I*)/FM electrodes to reduce interfacial resistance. The regions for n-type channels and n+-Si were formed in the Si substrate by using ion implantation of phosphorus (P) and arsenic (As), respectively, and post-rapid thermal annealing. We are confining spin transport in the active region of the n-type channel. The doping densities $N_d$ in the n-Si channel layer for the spin-injection devices were from ~$5\times10^{18}$ to ~$5\times10^{19}\,cm^{-3}$. For both the spin-injection devices and the *STS*-MOSFETs, the doping density in the n+-Si layers was 4–$5\times10^{20}\,cm^{-3}$. A tunnel barrier (MgO, $SiO_x$ or MgO/$SiO_x$) was formed on the Si surface and followed by deposition of a ferromagnetic layer in a UHV sputtering system. The $SiO_x$ layers were formed *in situ* by radical oxidation methods in the chamber. The FM and MgO layers were deposited by DC and RF magnetron sputtering, respectively. The MTJ stack for *STS*-MOSFETs consists of $(Co_{50}Fe_{50})_{80}B_{20}$ (CoFeB)/MgO/$Co_2FeAl_{0.5}Si_{0.5}$ (CFAS)/Ru/$Co_{50}Fe_{50}$ (CoFe)/$Ir_{22}Mn_{78}$/Ru/Ta. The detail structures of all samples are shown in Table 1. The estimated $SiO_x$ thickness obtained by transmission electron microscopy (TEM) image is 1.0 nm for the condition of the radical plasma oxidization of 50 s. A large MTJ and a small MTJ were microfabricated on the n+-Si regions by using photolithography, Ar ion milling and reactive-ion etching. The dimensions of the large and small MTJs, used to confirm the *STS*-MOSFET device operation are $0.35\times1.5\,\mu m^2$ and $0.3\times0.8\,\mu m^2$, respectively. Details of the processing for the MTJs are described elsewhere [21]. Current–voltage (*I*–*V*) measurements, non-local signal measurements and local MR measurements were carried out for spin-injection devices. Read/write operations and detailed read and write characteristics of the *STS*-MOSFET were investigated for the back-gate *STS*-MOSFETs.

## 3. Junction resistance of FM/I/Si diodes

For highly efficient spin injection and detection into semiconductors, tunneling conduction across the tunnel barriers is very important [22,23]. To obtain spin-dependent transport in a Si channel, interface resistances $r_b^*$ of n+-Si/I/FM should be in a specific range depending on the spin-diffusion length in Si as shown below: [22]

$$r_N\left[\Omega\cdot\mu m^2\right]\cdot\left(\frac{t_N[\mathrm{nm}]}{l_{sf}^{Si}[\mathrm{nm}]}\right)^2\cdot\left(\frac{W[\mu m]}{w[\mu m]}\right)<<r_b^*<<r_N\left[\Omega\cdot\mu m^2\right]\cdot\left(\frac{W[\mu m]}{w[\mu m]}\right), \quad (1)$$

where $r_N$ is the spin resistance of Si channel, $t_N$ is the channel length, $l_{sf}^{Si}$ is the spin-diffusion length in [nm], and W, w is a width of magnetic bar and the Si mesa depth in [μm], respectively. A typical

**Table 1**
Details of the structure of the films for all samples used in this work.

| Sample ID# | Dopant ion in Si substrate | Doping concentration | Structure of the films |
|---|---|---|---|
| Diode 1 | P (Phosphorus) | $5\times10^{18}$ | Plasma10 s/MgO0.4 nm/CoFeB6 nm/Ru24 nm |
| Diode2 | As (Arsenic) | $4\times10^{20}$ | Plasma10 s/MgO0.4 nm/CoFeB6 nm/Ru24 nm |
| Diode3 | P (Phosphorus) | $5\times10^{19}$ | MgO0.6 nm/CoFe6 nm/Ru24 nm |
| Diode4 | As (Arsenic) | $4\times10^{20}$ | MgO0.6 nm/CoFe6 nm/Ru24 nm |
| Diode5 | P (Phosphorus) | $4\times10^{20}$ | MgO0.6 nm/CoFeB6 nm/Ru20 nm |
| Diode6 | As (Arsenic) | $5\times10^{20}$ | MgO0.6 nm/CoFeB6 nm/Ru20 nm |
| Diode7 | As (Arsenic) | $5\times10^{20}$ | MgO0.5 nm/CoFeB6 nm/Ru20 nm |
| Diode8 | P (Phosphorus) | $5\times10^{18}$ | MgO1 nm/CFAS6 nm/Ru24 nm |
| Diode9 | As (Arsenic) | $4\times10^{20}$ | MgO0.6 nm/CFAS6 nm/Ru24 nm |
| Diode10 | As (Arsenic) | $5\times10^{20}$ | Plasma20 s/CoFeB6 nm/Ru24 nm |
| Diode11 | As (Arsenic) | $5\times10^{20}$ | Plasma50 s/CoFeB6 nm/Ru24 nm |
| Diode12 | As (Arsenic) | $5\times10^{20}$ | Plasma100 s/CoFeB6 nm/Ru24 nm |
| Diode13 | As (Arsenic) | $5\times10^{20}$ | Plasma200 s/CoFeB6 nm/Ru24 nm |
| Diode14 | As (Arsenic) | $4\times10^{20}$ | Plasma60 s/CoFeB6 nm/Ru24 nm |

| Sample ID# | Substrates | Structure of the films |
|---|---|---|
| MTJ 1 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.3 nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| MTJ2 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.4 nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| MTJ3 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.4 nm/CoFe0.4 nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| MTJ4 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.4 nm/Fe0.4 nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| MTJ5 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.4 nm/Co0.4 nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| MTJ6 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.4 nm/CoFeB0.4 nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| MTJ7 | $SiO_2$/Si | Ta5 nm/CoFeB30 nm/MgO1.4 nm/CoFeB5 nm/IrMn10 nm/Ru7 nm |
| MTJ8 | Si As-doped($4\times10^{20}$) | MgO-wedge buffer 1–5 nm/CFAS30 nm/$MgO_2$ nm/CFAS5 nm/IrMn10 nm/Ru7 nm |
| *STS*-MOSFET | Silicon-on-insulator (SOI) | Plasma 50 s/CoFeB3.5 nm/MgO0.85 nm/CFAS5 nm/Ru0.9 nm/CoFe2.5 nm/IrMn10 nm/Ru10 nm |