Thin Solid Films 519 (2011) 6525–6529

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Capacitance–voltage characterization of silicon oxide and silicon nitride coatings as passivation layers for crystalline silicon solar cells and investigation of their stability against x-radiation

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ARTICLE INFO

Article history:
Received 23 June 2010
Received in revised form 21 December 2010
Accepted 17 April 2011
Available online 22 April 2011

Keywords:
Capacitance–voltage
Interface traps
Plasma-enhanced chemical vapor deposition
Silicon oxide
Silicon nitride
Solar cells
Passivation
X-ray induced degradation

ABSTRACT

In this work capacitance–voltage measurements of three different dielectric layers, thermal silicon oxide, plasma enhanced chemical vapor deposited (PECVD) silicon oxide, and PECVD silicon nitride, on p-type silicon have been performed in order to obtain characteristics as the energy distribution of the interface trap density and the density of fixed charges. Spatially resolved capacitance–voltage, ellipsometry and lifetime measurements revealed the homogeneity of layer and passivation properties and their interrelation. Additionally lifetime measurements were used to evaluate x-radiation induced defects emerged during electron beam evaporation for sample metallization.

1. Introduction

The photovoltaic industry is driven by the need of cost reduction and efficiency improvement. A candidate for high efficiency solar cells is the so called PERC (passivated emitter and rear cell) concept [1,2]. In this cell design and related cell structures, the rear side of the solar cell is covered with a passivation layer reducing the surface recombination of photo generated excess carriers, allowing for higher short circuit currents and open circuit voltages, thus improving the cell efficiency. As passivation layer for the rear side, thermal SiO_2 has been the standard for many years in high efficiency solar cells made from mono crystalline silicon. Recent research has focused on replacing the thermal SiO_2 by layers manufactured by plasma enhanced chemical vapor deposition (PECVD), since processing time and thermal budget would be reduced by this approach. Subsequently, an adaption of the PERC concept to solar cells made of cheaper multicrystalline silicon material in an industrial production would be facilitated [3].

As the two fundamental surface passivation principles are the reduction of the interface traps and the implementation of a field-effect passivation due to electrical charges [4], the interface between silicon wafer and passivation layer as well as the charges in the passivation layer are of particular interest. A suitable method for investigating dielectric layers, surface and interface properties are capacitance–voltage (CV) measurements. In this article, PECVD hydrogenated silicon nitride, PECVD silicon oxide and thermal silicon oxide layers are studied. The former is widely used as antireflection coating and has also been investigated for usage as a passivation layer in crystalline silicon solar cell technology [5,6]. A very promising approach for rear side passivation is the combination of PECVD based silicon oxide and silicon nitride, which has been successfully integrated in cell structures [7,8].

Metal-insulator-semiconductor (MIS) diodes serve as a model structure to determine the density of interface traps D_{it} [9]

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE} \tag{1}$$

and fixed charges N

$$N = \frac{Q_{diel}}{q} \tag{2}$$

with charge density Q_{it} trapped in interface states, charge density Q_{diel} in the dielectric layer, corresponding energy level E and elementary charge q.

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0040-6090/$ – see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2011.04.107

The effective minority carrier lifetime t_{eff} is taken as a measure for the surface passivation quality on high quality (Fz) silicon material.

2. Experimental details

2.1. Sample preparation

The metal-insulator-semiconductor (MIS) structures were prepared as shown in Fig. 1. The wafers, single sided covered with the according dielectric layer, firstly received a short dip in 1% HF solution. Subsequently, the back contacts were fabricated by means of electron beam evaporation. Afterwards the front side dielectric was also covered with evaporated aluminum and the contacts were structured using a photolithographical lift-off process with a front contact size of 1 mm^2 and 0.1 mm^2. To anneal electron beam gun induced defects the CV samples were tempered for six minutes at 400 °C in a belt furnace in air.

Three different dielectric layers have been investigated: A thermal silicon oxide (thermal SiO) was grown on p-doped (100) oriented Cz-wafers with a resistivity of 5 Ω cm. For the fabrication of the MIS structure, the thermal oxide was removed on one side by etching in 5% HF solution. PECVD silicon oxide (SiO) and PECVD silicon nitride (SiN) were deposited on p-doped (100) oriented Fz-wafers of 1 Ω cm. The SiO and SiN were grown in a 13.56 MHz direct plasma PECVD reactor by the use of SiH_4 and N_2O for SiO and SiH_4, H_2, NH_3 for SiN [10]. Before the evaporation of the contacts, the SiN sample was fired at a peak furnace temperature of 830 °C in order to obtain better hydrogen passivation [11] and to decrease leakage currents. For lifetime samples the PECVD layers were symmetrically deposited on both sides of the wafers.

2.2. CV measurements

Capacitance–voltage (CV) measurements were performed using the combined high-frequency (hf) low-frequency (lf) method [12]. Following this approach, D_{it} was determined by the stretch out between hf and lf CV curves in the depletion region due to interface traps as

$$D_{it}\left(V_g\right) = \frac{C_{diel}}{q}\left[\frac{C_{lf}\left(V_g\right)}{C_{diel}-C_{lf}\left(V_g\right)} - \frac{C_{hf}\left(V_g\right)}{C_{diel}-C_{hf}\left(V_g\right)}\right] \quad (3)$$

where C_{lf} and C_{hf} are the measured low-frequency and high-frequency capacitance values, V_g is the applied DC bias voltage and C_{diel} the capacitance of the dielectric layer. C_{diel} is the measured capacitance value biasing the sample to accumulation. It is independent of the frequency. The sensitivity of the used device allows the determination of D_{it} above $1 \cdot 10^9$ cm^2 eV^{-1}. Berglund's integral gave the relation between surface potential and gate voltage leading to D_{it} as a function of energy [13]. N was extracted from the shift of the flat band voltage, which was deduced from the flat band capacitance. The work function difference of aluminum and silicon was taken to be −0.85 V [14]. The capacitance itself was determined by a phase-sensitive measurement of the impedance using a HP 4284A LCR Bridge.

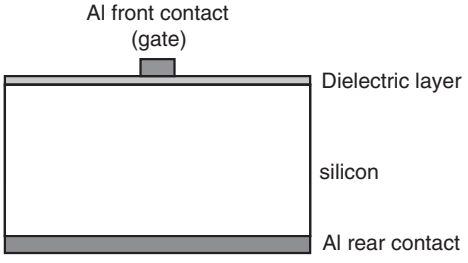

Fig. 1. Schematic representation of the MIS structure used in this work. Rear and front contacts were fabricated by electron beam evaporation of aluminum. The gate voltage V_g is defined >0 when the gate is charged positively with respect to the rear contact.

The MIS diodes were measured in 4-Terminal Pair (4TP) [15] configuration in order to minimize mutual coupling. The use of four coaxial cables ensured the separation of the voltage sensing from the current path. To reduce residuals existing in the measurement setup an open/short compensation was performed in which residual impedance and stray admittance are modeled in a linear network [15].

The samples were fixed by vacuum on a copper plate which also served as rear contact. The gate was contacted via a contact needle and a micromanipulator.

Low-frequency CV curves can be recorded, depending on the sample, in the range of 100 Hz to 10 kHz. Here, the low frequency was 2 kHz for the PECVD silicon oxide and 1 kHz for the PECVD silicon nitride and the thermal oxide. High-frequency CV curves were taken at 1 MHz for all samples. The amplitude of the AC signal was 15 mV. For obtaining a low-frequency CV curve, the sweep rate of the DC bias voltage must be slow enough to ensure that the minority carriers and interface traps can follow. The sweep rate of the DC bias voltage was kept at 0.02 V/s. All the samples were measured from inversion to accumulation and the homogeneity of D_{it} and N was investigated by measuring CV curves on several gate contacts on the samples.

2.3. Additional measurements

The thickness of the dielectric layers and their refraction index were spatially resolved measured with a Sentech SE502 single wavelength ellipsometer. The symmetrical lifetime samples were used to measure minority carrier lifetime maps by the transient microwave photoconductance decay (μPCD) method with a Semilab WT2000 instrument. An excitation of $1.5 \cdot 10^{12}$ photons per laser pulse and a bias illumination of 0.5 suns were used.

In order to investigate the influence of x-radiation during the aluminum evaporation process on the surface passivation quality, measured lifetime samples were covered on one side with adhesion foil. This side of the samples was afterwards exposed to aluminum deposition by means of electron beam evaporation with the same process parameters as used for the metallization of the MIS samples. The foils were subsequently peeled off together with the evaporated metal and a second lifetime mapping was performed. Afterwards, an annealing step as for the MIS structures was conducted and a last lifetime map taken.

3. Results and discussion

3.1. Interface trap distribution and fixed charges

D_{it} as a function of energy within the band gap for the three samples is shown in Fig. 2. The typical u-shaped energy distributions for the Si–SiO_2 interfaces [16] as well as for the Si–SiN interface are observable.

The strong increase of D_{it} toward the band edges has been measured by P.V. Gray and D.M. Brown [17] and W. Fahrner and A. Götzberger [18] for Si–SiO_2 interfaces. Castagné et al. proposed an interpretation of this observation [19] based on the presence of a thin non stoichiometric oxide layer between Si and SiO_2. This layer is thought to contain mobile charges which are able to capture both holes and electrons and by that to change the surface potential. Both PECVD silicon oxide and PECVD silicon nitride show a similar increase. For further discussion we focus on the interface traps in the middle of the band gap since D_{it} near midgap is most crucial for carrier lifetime [20].

Commonly D_{it} at midgap is used to evaluate the interface trap density of a MIS capacitor. Some authors refer to the minimum value