



The characteristics of fluorinated polycrystalline silicon oxides and thin film transistors by CF₄ plasma treatment

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ABSTRACT

This study describes a simple fluorinating technique by the tetrafluoromethane (CF₄) plasma treatment to form fluorinated polyoxides and polycrystalline silicon thin film transistors (TFTs). In comparison with the non-fluorinated device, the fluorinated polyoxides and devices exhibit a higher breakdown field (>8 MV/cm), low charge trapping rates, low off-state current, and low trap states. Furthermore, the performance and reliability of the fluorinated devices are also improved by the CF₄ plasma treatment. This is due to the fact that the incorporated fluorine can break strain bonds to form stronger silicon–fluorine (Si–F) bonds to passivate the generation of interface and trap states existing near the polyoxide/polysilicon interface and grain boundaries.

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1. Introduction

The oxides grown on n+ doped polysilicon, that is, polyoxides, have been widely used as the interlayer dielectrics [1,2] for flash memory and low temperature polycrystalline silicon thin film transistors (LTPS TFTs) application. However, polyoxides have drawbacks such as higher leakage current and a lower breakdown electric field than oxides grown on single crystal silicon. To obtain good data retention characteristics, polyoxides with low conductivity and high breakdown fields have long been sought [3–5].

Recently, deposited chemical vapor deposition dielectrics have been considered to be a very promising alternative since they are deposited on the polysilicon layer without polysilicon consumption that increases interface roughness. However, the oxides deposited by the plasma enhancement chemical vapor deposition (PECVD) at a low temperature of about 300 °C potentially have poor electrical properties and more oxide trap charges due to a large number of dangling bonds. Furthermore, PECVD-oxides grown on N+ polysilicon have also exhibited poor characteristics due to many grain boundary trap states and interface states existing in the oxide network and polyoxide/polysilicon interfaces. Therefore, it is critical to reduce the trap states for polyoxides and TFTs effectively.

The oxides incorporated with fluorine have also been reported to cause local strain stress relaxation and less interface states because of

the passivation of interface defects such as dangling bonds and strain bonds [6–8]. Furthermore, the fluorine incorporation does not only improve electrical characteristics such as ON-current, subthreshold swings, and mobility, but it also improved the hot-carrier immunity of the TFTs. This is due to the fact that fluorine can passivate dangling bonds and strain bonds more uniformly to reduce the trap states in the band tail and midgap [9–12].

Previous study has demonstrated a CF₄ plasma treatment on solid-phase-crystallized (SPC) poly-Si thin film transistors, which can provide an effective and process compatible method to introduce fluorine atoms into poly-Si film to fabricate high-performance as well as high-reliability poly-Si TFTs [13]. Furthermore, high-k Pr₂O₃ material as gate dielectric combined with CF₄ plasma passivated poly-Si poly-Si TFTs has been demonstrated [14]. The incorporation of fluorine atoms by CF₄ plasma treatment can also improve the electrical characteristics and reliability of poly-Si Pr₂O₃ TFTs against hot-carrier stressing, which is due to the formation of stronger Si–F bonds in place of weak Si–H bonds in the poly-Si channel and at the Pr₂O₃ gate dielectric/poly-Si interface. However, few studies reported the CF₄ plasma treatment applied in the polyoxide grown on polycrystalline silicon.

In our study, we propose a simple fluorinating technique by employing the tetrafluoromethane (CF₄) plasma treatment to fabricate the fluorinated polyoxides on polycrystalline silicon, which exhibit better polyoxide quality and performance with higher breakdown field (>8 MV/cm), low charge trapping, low off-state current, and low trap state densities. Furthermore, the performance and reliability of the fluorinated thin film transistors are also improved by the CF₄ plasma treatment.

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2. Experiments

2.1. Fluorinated polyoxide process

In this study, aluminum/polyoxide/n⁺-polysilicon capacitor structures were fabricated by the following process sequence. P-type Si wafers with a thickness of 600 nm were thermally oxidized. The polysilicon film with a thickness of 300 nm was then deposited by a low-pressure chemical vapor deposition (LPCVD) at a substrate temperature of 625 °C. The polysilicon film as a bottom electrode was implanted with phosphorous at $5 \times 10^{15} \text{ cm}^{-2}$ dosage and 30 keV. To activate the dopant, a rapid thermal process was performed in N₂ ambient only for 30 s at a temperature of 950 °C. The sheet resistance of the polysilicon film was 81 Ω/square.

After removing the native oxide by dipping in diluted hydrofluoric acid (HF) solution, the samples were subjected to the CF₄ plasma treatment conducted in a plasma enhancement chemical vapor deposition (PECVD) system at 300 °C for 30 s and 1 min with a pressure of 80 Pa and a power of 15 W. A polyoxide with a thickness of 50 nm was in-situ deposited to serve as the gate insulator using SiH₄ and N₂O gas mixture at 300 °C in the same chamber. The samples were then densified at 500 °C for 15 min in an O₂ ambient. A 300 nm thick aluminum film was evaporated on a polyoxide and patterned as the gate electrode. Fig. 1(a) and (b) shows the schematic diagram of the polyoxide capacitors and detailed process flow.

2.2. Fluorinated thin film transistors process

At first, the thin film transistors were fabricated on thermally oxidized silicon wafers. An amorphous-silicon (α-Si) film of about 100 nm was initially deposited at 550 °C by LPCVD using pure SiH₄ gas and then furnace-annealed at 600 °C for 24 h in N₂ ambient to recrystallize the silicon films from amorphous silicon transformed into polycrystalline silicon. After the crystallization of the α-Si layer, the silicon active regions were patterned and defined by photolithography and etch processes. The samples were then subjected to the CF₄ plasma treatment conducted in a PECVD system at 300 °C for 30 s and 1 min with a pressure of 80 Pa and a power of 15 W. The oxide with a

thickness of 40 nm was in-situ deposited by the PECVD system to serve as the gate insulator using SiH₄ and N₂O gas mixture at 300 °C in the same chamber. Another 200 nm thick polysilicon film was deposited at 620 °C and then patterned as the gate area. A self-aligned phosphorus ion implantation with a dose of $5 \times 10^{15} \text{ cm}^{-2}$ and 40 KeV energy was used to dope the drain, source, and gate areas. The dopants were then activated at 600 °C for 12 h. After 250 nm thickness oxide was deposited by PECVD system as the passivation layer, the contact holes were opened and the aluminum films were deposited and then defined.

The oxide thickness was determined at a high-frequency (1 MHz) using the Keithley capacitance–voltage (C–V) measurement; and the oxide dielectric constant was about 3.9. The amount of fluorine in the polyoxide/polysilicon interface was estimated using a ION-TOF SIMS IV (time-of-flight secondary ion mass spectrometry) with Cs⁺ as primary ions. Si wafer implanted with BF₂ at a $1 \times 10^{15} \text{ cm}^{-2}$ dosage was used as standard sample for quantification.

The morphology of the polyoxide/polysilicon interface was studied by Veeco D5000 atomic force microscope (AFM) operated in tapping mode using an Applied Nano silicon tip with a 50 N/m spring constant. Scan rate used was 1 Hz, scan area was $2 \mu\text{m} \times 2 \mu\text{m}$, and the set engagement ratio was 80%. In order to reveal the polysilicon surface for the AFM measurements, the polyoxide layer was removed by wet etching in the buffered HF acid. The electrical characteristics of the polyoxides and thin film transistors were measured using the HP4156C semiconductor parameter analyzer.

3. Results and discussion

3.1. Fluorinated polyoxides

Fig. 2 shows the secondary ion mass spectroscopy (SIMS) profiles of fluorine, oxygen, and silicon for the fluorinated polyoxide with CF₄ plasma treatment. It is clear that most of the fluorine ions pile up near the polyoxide/polysilicon interface and move from the original position to diffuse and incorporate into the polyoxide. The incorporated fluorine can break strain bonds to form stronger Si–F bonds in the gate oxide network to improve gate oxide quality and electrical characteristics. Maegawa et al. [10] also reported that the fluorine atoms implanted into the gate poly-Si moved from the original position and segregated into the neighboring gate oxide and bottom oxide during post annealing. This segregation suggests that some changes occurred in the oxide. In our study, the distribution of fluorine in the polyoxide was formed by diffusion during post annealing (500 °C, 15 min, in O₂ ambient), and the fluorine ions diffused from the polyoxide/polysilicon interface and incorporated

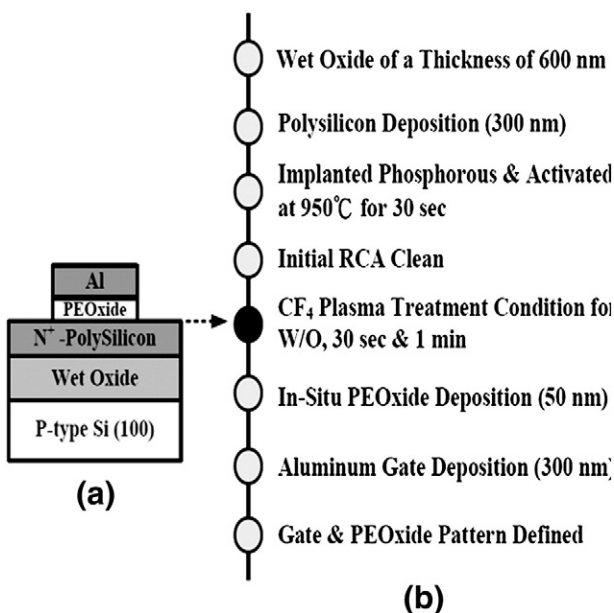


Fig. 1. (a) The schematic diagram of the fluorinated polyoxides. (b) The process flow of the fluorinated polyoxides with CF₄ plasma treatment.

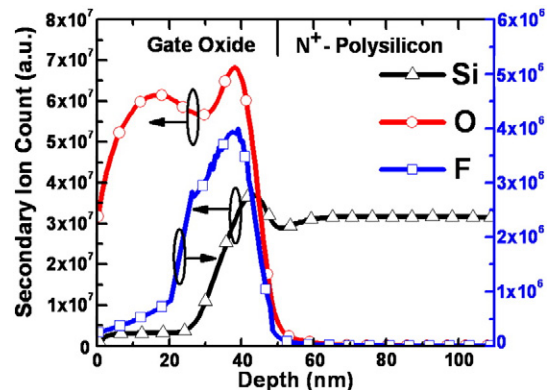


Fig. 2. The secondary ion mass spectroscopy (SIMS) profile analysis of silicon, oxygen, fluorine for the fluorinated polyoxide with CF₄ plasma treatment.

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