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Amorphous/crystalline silicon heterojunction solar cells with varying i-layer thickness ☆

M.R. Page *, E. Iwaniczko, Y.-Q. Xu, L. Roybal, F. Hasoon, Q. Wang, R.S. Crandall

National Renewable Energy Laboratory (NREL), 1617 Cole Blvd., Golden, CO 80401, USA

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ABSTRACT

We study the effect on various properties of varying the intrinsic layer (i-layer) thickness of amorphous/crystalline silicon heterojunction (SHJ) solar cells. Double-side monocrystalline silicon (c-Si) heterojunction solar cells are made using hot-wire chemical vapor deposition on high-lifetime n-type Czochralski wafers. We fabricate a series of SHJ solar cells with the amorphous silicon (a-Si:H) i-layer thickness at the front emitter varying from 3.2 nm (0.8xi) to ~96 nm (24xi). Our optimized i-layer thickness is about 4 nm (1xi). Our reference cell (1xi) performance has an efficiency of 17.1% with open-circuit voltage (V_{oc}) of 684 mV, fill factor (FF) of 76%, and short-circuit current density (J_{sc}) of 33.1 mA/cm^2. With an increase of i-layer thickness, V_{oc} changes little, whereas the FF falls significantly after 12 nm (3xi) of i-layer. Transient capacitance measurements are used to probe the effect of the potential barrier at the n-type c-Si/a-Si interface on minority-carrier collection. We show that hole transport through the i-layer is field-driven transport rather than tunneling.

1. Introduction

When applied to the full area of a crystalline silicon (c-Si) wafer, thin hydrogenated a-Si:H layers have an excellent passivation capability and enable good carrier transport. These layers when bifacially applied can serve as both the front emitter and back-surface-field (BSF) contact, as demonstrated in high-efficiency silicon heterojunction (SHJ) solar cells such as Sanyo's 23% double-heterojunction "HIT" solar cells [1]. Because of the band mismatches between a-Si:H and c-Si, potential steps hinder charge transport. This is most noticeable with n-type c-Si. To better understand the role of the front-junction buffer i-layer, we fabricated SHJ solar cell devices having i-layers with varying thickness using all hot-wire chemical vapor deposition (HWCVD). Electronic performance of the solar cells was characterized by solar-simulation-lighted current and voltage measurements (LIV), as well as internal quantum efficiency (IQE). We used a capacitance transient technique to measure the electrical response characteristics of the i-layer and characterize the charge transport through the i-layer. We show that our measurements support the conclusion that the dominant transport mechanism for minority holes collected through the i-layer is by transport, rather than tunneling through the i-layer.

2. Experimental details

Fig. 1 illustrates the simplistic double-side SHJ device structure we employ in this study of the i-layer transport. We use HWCVD for deposition of all our doped and intrinsic a-Si:H films on the c-Si wafer sample. HWCVD offers the important advantage of deposition with low ion bombardment at the critical c-Si interface. Excellent surface passivation is achieved using a thin i-layer to create an abrupt interface between the c-Si/a-Si:H with no epitaxial growth, as seen in the high-resolution transmission electron microscope image in the Fig. 1 inset [2]. Unfortunately, commonly doped amorphous silicon absorbs in the visible spectrum, leading to parasitic absorption in the blue-wavelength region and requiring that we thin the a-Si:H layers as much as possible without sacrificing electrical performance.

In this study, we purposely thicken the i-layer to study the carrier transport through it. We assume that for our thickest i-layer, ~96 nm (24xi), we have similar material properties to our standard optimized i-layer thickness (1xi), with all other parameters being constant. All films were deposited on a 25-mm × 45-mm wafer sample cleaved from the same commercially available planar n-type Czochralski (CZ)

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* Corresponding author.
E-mail addresses: Matthew.Page@nrel.gov (M.R. Page), Eugene.Iwaniczko@nrel.gov (E. Iwaniczko), Yueqin.Xu@nrel.gov (Y.-Q. Xu), Lorenzo.Roybal@nrel.gov (L. Roybal), Falah.Hasoon@nrel.gov (F. Hasoon), Qi.Wang@nrel.gov (Q. Wang), Richard.Crandall@nrel.gov (R.S. Crandall).

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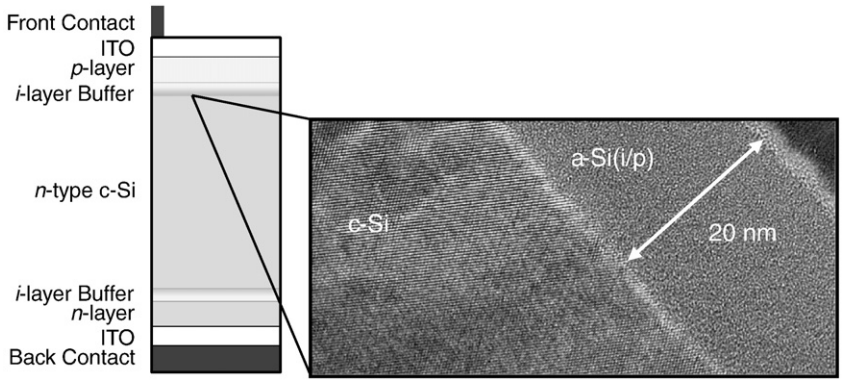

Fig. 1. Schematic of double-side SHJ solar cell and high-resolution transmission electron microscopic image of abrupt cSi(p)/aSi:H(i/p).

<100>-oriented, 1.6-Ωcm, electronic-grade wafer. We carefully cleaned all the samples together using our standard cleaning procedure [3]; the resultant chemical oxide preserves a high-quality c-Si surface until our final dilute 2.5% hydrofluoric acid (HF) oxide flush to strip the protective oxide cap before loading into the vacuum deposition system. For SHJ devices, the junctions are formed at the c-Si/a-Si:H interfaces, so it is critical to have a clean interface just prior to a-Si:H deposition. By minimizing or eliminating contamination or defects on the surface, we ensure good junction and contact interfaces.

Our HWCVD deposition systems are capable of i- , n-, and p-layer deposition in separate chambers, but only with an air break between i- and n-layer depositions. Our optimized a-Si:H layer deposition conditions are reported elsewhere [2–4]. After reaching a base pressure below 5×10^{-8} torr in the HWCVD deposition chamber, all depositions consist of a substrate heating period under high vacuum followed by gas dynamic stabilization and controlled deposition using a shutter. Our hot-wire filament materials are tantalum for the i-layer or tungsten for the doped layers. Thermally evaporated indium tin oxide (ITO) is used for the back contact and top emitter contact to the a-Si:H, as well as the single-layer antireflection coating. Metallization of both sides is by electron-beam evaporation of the Ti/Pd/Ag/Pd stack.

We investigate hole transport through the a-Si:H i-layer by concentrating on the low-temperature region where thermal emission over the barrier is too slow to compete with transport through the i-layer. Capacitance is well suited to study hole transport through the band offset because it measures charge. We produce holes at the interface with a monochromatic light flash and then follow their loss in the dark via a change in the capacitance. At low enough temperature, thermal emission over the potential step is too slow to compete with transport through the barrier. Thus, measuring a hole escape-transient at low temperature should probe the latter process.

3. Results and discussion

3.1. Device characteristics

For LIV performance characteristics in Table 1, the difference in fill factor (FF) is influenced by the thickness of the i-layer because minority-carrier transport is affected by the i-layer thickness. There are other factors influencing the FF of these devices such as ITO thickness, ITO sheet resistance, contact resistances, and front-contact metallization. Except for very thick i-layer films, the impact of the thick buffer layer is minimal in comparison to the device fill factor. We were able to measure fill factors on the order of 78% for i-layer thicknesses 2xi or thinner. For the other devices, if we calculate the efficiency if we had reached 78% FF, then for all devices except the 24xi sample, we would have an average efficiency of 16.7%. Transport through the thick i-layer is most likely responsible for the drop in FF beginning at 3xi thickness. The open-circuit voltage (V_{oc}) is consistently above 670 mV, indicating that the properties of the junction and back contact are similar.

For IQE in Fig. 2, we see that the blue response of all our SHJ cells compared to the NREL p-type diffused-junction solar cell is poor. Current is lost in the front of the SHJ cell structure due to absorption in the a-Si:H p- and i-layers, as demonstrated by greater loss in the blue as the thickness of the i-layer increases. Normally, the IQE response in the red region of the spectrum is not influenced by external electrical properties except in the case of the 24x i-layer. For very thick i-layers, the red response of the cell is decreased although the bulk properties of the c-Si sample have not; this indicates that the electrical transport to detect the carriers has degraded.

3.2. Electrical properties of the i-layer

Because of the potential step at the c-Si/a-Si:H interface, a hole must be thermally excited over or pass through the i-layer before it recombines with a photoexcited electron. At low temperature, transport through the i-layer would be the dominate mode. Thermal emission depends only on the height of the potential step and temperature, whereas tunneling or hopping transport depends both on the step and the i-layer thickness. Once the hole reaches the p-layer, it is extracted through dielectric relaxation and recombines in the ITO.

Fig. 3 shows a capacitance transient represented by ΔC/C, which is a measure of the minority carriers (holes) present after the light is turned off. The initial values are a measure of the holes transported to the interface. Beginning at about 0.4 ms, the hole density decreases to 0 in about 10 ms, which represents the point when all the holes have escaped through the i-layer and are collected. The transients in Fig. 3 are virtually identical, indicating the absence of a significant thermal

Table 1
Summary of SHJ solar cell device performance under AM1.5 LIV conditions for varying i-layer thickness.

a-Si:H i-Layer Thickness	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
0.8xi [3.2 nm]	672	31.9	74.8 (78)	16 (16.7)
1xi [4 nm]	681	32.4	78	17.2
2xi [8 nm]	671	31.6	78.4	16.6
3xi [12 nm]	680	32	71 (78.4)	16.6
6xi [24 nm]	673	31.9	59.1 (78)	12.7 (16.7)
24xi [96 nm]	680	12.5	18.5 (78)	1.6 (6.6)