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Trapping properties of sputtered hafnium oxide films: Bulk traps vs. interface traps

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ABSTRACT

The purpose of this work is to investigate the influence of the spatial distribution of traps on the electrical characteristics of hafnium oxide films deposited by physical vapor deposition. Samples were Al gated metal-oxide-semiconductor capacitors with hafnium oxide films deposited on SiO_2 layer thermally grown on Si. During capacitance–voltage measurements large hysteresis, up to 10 V, are observed in all samples. It is shown that depending on the hafnium oxide deposition conditions, the spatial distribution of the traps responsible for the hysteresis can be either two dimensional (interface/border traps) or three dimensional (bulk traps).

1. Introduction

The metal-oxide-nitride-oxide-semiconductor (MONOS) structure [1] has a good potential to replace floating gate type memory. Retention properties of MONOS devices are in general higher than floating gate ones since a single defect in the tunneling oxide layer of the former discharges the memory only locally. As a consequence scaling of tunneling oxide thickness is more aggressive in MONOS type memories. High-k materials as a charge storage layer appear more attractive than nitride layers since they provide a larger physical thickness for the same equivalent oxide thickness (EOT) leading to a higher trap number. Hafnium oxide is a good high-k candidate material and it will be considered in the present work. Many different deposition techniques have been used to form hafnium oxide, namely metal-organic chemical vapor deposition [2], chemical vapor deposition [3] , atomic layer deposition [4] , molecular beam epitaxy [5] and sputtering [6]. In this work the charge trapping properties of hafnium oxide deposited by physical vapor deposition (PVD) from a pure hafnium oxide target will be presented. Hafnium oxide is deposited over a SiO_2 layer thermally grown on a Si substrate. The effect of deposition conditions, hafnium oxide layer thickness and SiO_2 layer thickness onto the ability of the hafnium oxide layer to trap charges will be discussed. An interesting feature we would like to address in this work is the position of the trapping centers within the HfO_2 film. Are these bulk traps or are they situated nearby the interface of the high-k material with the tunneling oxide? Understanding how material deposition conditions can influence trapping centers distribution is of critical importance for memory applications.

2. Experimental details

Hafnium oxide films have been deposited from a high purity HfO_2 target by PVD, namely RF sputtering. Films were deposited on SiO_2, thermally grown using dry oxidation of silicon substrates at 850 °C. During all depositions the argon flux was at 60 sccm, the pressure at $8\ 10^{-3}$ mbar, the deposition rate was kept constant at 0.1 /s at 200 W power and the thickness of the deposited film ranged between 10 and 30 nm. After deposition of the HfO_2 film, aluminum was evaporated and patterned to form MIS capacitors. The deposition parameters which are investigated in this work are the deposition temperature and deposition ambient. Details about the deposition conditions are presented in Table 1.

Electrical characterization was carried out by capacitance–voltage (C–V) measurements using an HP4284a. In order to characterize the trapping properties of the hafnium oxide films we have performed C–V measurements at room temperature on all samples under sweeping bias conditions of increasing amplitude (frequency 1 MHz, sweep rate 1 V/s). Namely, from 2 V→−2 V (backward sweep) and from −2 V→2 V (forward sweep), then 3 V→−3 V and −3 V→3 V, and so on until hard break down conditions of the dielectric are reached. No waiting time was applied between two consecutive

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Table 1
Fabrication details of the samples discussed in this work.

	Sample code						
	A	B1	B2	B3	I1	I2	I3
Substr. type	p	p	p	p	p	p	p
Nominal SiO_2 thick. (nm)	3.5	3.5	3.5	3.5	3.5	3.5	8
Nominal HfO_2 thick. (nm)	30	10	20	30	30	15	30
HfO_2 dep. Temp. (°C)	25	200	200	200	300	300	300
HfO_2 dep. Ambient	Ar	Ar:O_2 2:1	Ar:O_2 2:1	Ar:O_2 2:1	Ar:O_2 6:1	Ar:O_2 6:1	Ar:O_2 6:1
Post Deposition Annealing (PDA)	400 °C, N_2: H_2, 20 min.	no	no	no	no	no	no

sweeps. The probe light was kept on during each electrical measurement in order to ensure a good level of minority carrier concentration in inversion regime.

3. Results and discussion

3.1. General remarks

Reference samples with only the SiO_2 film as dielectric do not exhibit any hysteresis of the C–V characteristics as it is shown in the inset of Fig. 1. For the samples in Table 1, the hysteresis observed is counter clockwise indicating that charging from the Si substrate is predominant [7].

A common feature of all samples discussed in this paper is the similarity of their electrical characteristics regarding hysteresis and charge retention. As an illustrating example, in Fig. 1 the C–V characteristics for different amplitude of the bias sweep cycle are presented for sample A. Then, in Fig. 2 we present the flat-band voltage shift dependence upon the sweep amplitude as extracted from Fig. 1. Large hysteresis is observed for sweeps above 8 V. The upper branch (electrons storage) and lower branch (holes storage) of Fig. 2 present different turning points. From that figure it is clear that electron trapping starts above 7 V while hole trapping starts above 11 V. This asymmetry can be attributed to the following factors:

– The higher effective mass of the tunneling holes with respect to that of electrons [8].

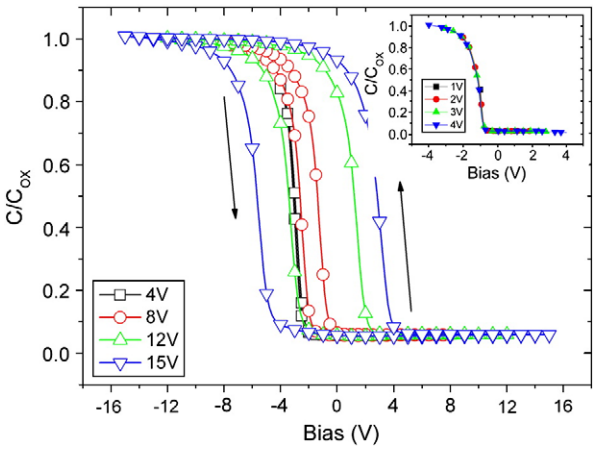

Fig. 1. C–V characteristics for sample A. Four sweeps are shown: 4 V(4 V → −4 V → 4 V) up to 15 V(15 V → −15 V → 15 V). Large hysteresis is observed above the 8 V cycle. In the inset: C–V characteristics for reference Al–SiO2–pSi structures. Four sweeps are shown: 1 V(1 V → −1 V → 1 V) up to 4 V(4 V → −4 V → 4 V). Neither hysteresis nor drift in the characteristics is found. From the capacitance in accumulation a value of 3.8 nm is extracted for the SiO2 layer thickness.

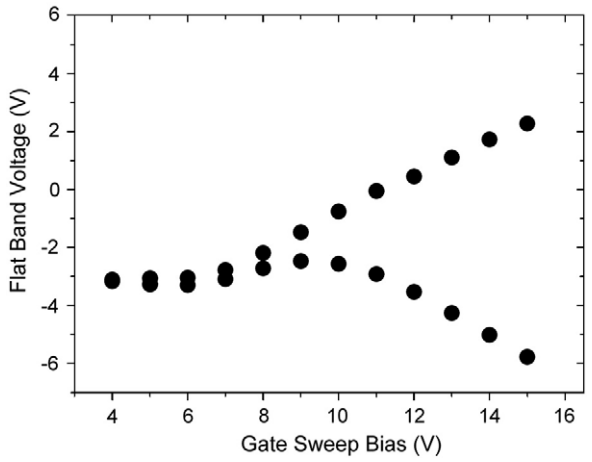

Fig. 2. Hysteresis plot showing the flat-band voltage dependence upon the bias sweep amplitude for sample A. The upper branch corresponds to backward sweeps.

– The higher potential barrier for holes with respect to electrons injected from silicon substrate. The hafnium oxide conduction band (CB) and the silicon oxide CB are 1.5 eV and 3.2 eV respectively above Si–CB while the hafnium oxide valence band (VB) and the silicon oxide VB are 3.4 eV and 4.6 eV below the Si VB [9].
– The energy distribution of the traps. Indeed, it is possible to explain the observed asymmetry assuming that electron traps are energetically closer to the Si conduction band than the hole traps to the Si valence band in such a way that electron traps are filled at lower electric field than hole traps. Theoretical [10] and experimental [2,11,12] studies show that this seems to be the case for hafnium oxide films.

In Fig. 3 the behavior of the devices under a pulsed regime is shown. Positive and negative pulses, with fixed duration and increasing height, are applied and each time a C–V measurement is performed to extract the flat-band voltage. In the case of pulses with 10 ms duration the hysteresis plot is very similar to the 2 s case with the only difference that in this case each pulse is slightly less effective [13] to charge all the traps available at each particular bias. However the loss of efficiency when using 10 ms instead of 2 s pulses is quite small. This result indicates a fast charging and discharging mechanism of the traps involved in the hysteresis and it justifies existing interest for MONOS-like memories based on hafnium oxide as the trapping layer [14,15].

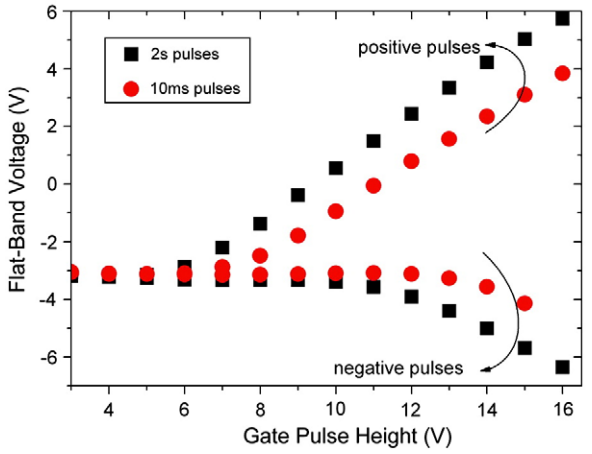

Fig. 3. Hysteresis plot under pulsed regime for sample A.