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Charge trapping characteristics in high-k gate dielectrics on germanium

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ABSTRACT

The results of a comparative study on the charge trapping/detrapping behavior in thin ZrO_2 and TiO_2 high-k gate dielectrics on p-Ge (100) under stressing in constant current (CCS, 1.02–5.1 C cm^{-2}) and voltage (CVS, −5 V to −7 V) at gate injection mode are presented. Stoichiometric thin films of ZrO_2 and TiO_2 have been deposited on p-Ge (100) using organometallic sources at relatively low temperature (<200 °C) by plasma enhanced chemical vapor deposition (PECVD) technique in a microwave (700 W, 2.45 GHz) plasma discharge at a pressure of 66.67 Pa. The effect of stressing on several important interfacial parameters, like, interface state density, fixed oxide charge, oxide charge centroids, and capture cross-section of traps etc. is reported.

1. Introduction

The continued scaling of Si CMOS devices has led to an increased attention to high-k gate dielectrics as replacements for SiO_2, where eventually the physical thickness (<10 A) of SiO_2 cannot be scaled further before gate oxide leakage becomes prohibitively large. As per the International Technology Roadmap for Semiconductors (ITRS) published in 2005, by the year 2010, the equivalent oxide thickness of 19 Å and gate leakage currents less than 7 pA/μm, will be required for the MOSFET devices for low standby power applications.

High-k dielectrics will be needed for high performance applications, which require very low equivalent oxide thicknesses of less than 1 nm. Much attention has been focused on various high-k dielectrics such as aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2) and hafnium oxide (HfO_2) as possible replacements for SiO_2, and various research groups have demonstrated high-k dielectrics scaled down to approximately t_{eq} ~10 Å with gate leakage currents significantly reduced compared to conventional SiO_2-based gates.

A major challenge of replacing SiO_2 with a high-k gate dielectric is the degraded channel mobility. Various approaches which enhance electron and hole mobilities, such as the use of strained silicon–germanium (SiGe) on Si, [1] or strained-Si on relaxed buffer SiGe layers [2] are now available. However, bulk Ge has recently received renewed attention as a possible replacement for Si in high-k CMOS devices, because of its higher electron (2.5X) and hole (4X) bulk mobility relative to that of Si allows for the prospect of improved MOSFET channel mobility, while maintaining the potential to continue aggressive device scaling.

However, many challenges remain to make high-k on Ge work, such as (i) the presence of traps and fixed charges in the film or at the interfaces, leading to significant flat-band voltage shifts and voltage bias instability; (ii) reliability issues as channel hot carriers and carriers from gate tunneling traverse the gate dielectric resulting in trap generation; and (iii) the degradation of carrier mobility of carriers in the MOSFET channel.

In this work, we have made a comparative study on the charge trapping/detrapping behavior in thin ZrO_2 and TiO_2 high-k gate dielectrics on p-Ge (100). Ultra thin layers of high-k dielectrics have been deposited using organometallic sources at a relatively low temperature (<200 °C) by plasma enhanced chemical vapor deposition (PECVD) technique in a microwave (700 W, 2.45 GHz) plasma discharge. MIS capacitors fabricated using the high-k dielectrics have electrically characterized for reliability studies under both the constant current (CCS at 1.02 C.cm^{-2} to 5.10 C.cm^{-2}) and voltage (CVS at −5 V to −7 V) stressing in gate injection mode. The effect of stressing on several important interfacial parameters, like, interface state density, fixed oxide charge, and capture cross-section of traps etc. have been studied.

2. Experimental

The Ge substrate (100) used was B-doped p-type wafers with a resistivity of 25–29 Ω-cm. We have used dry chemical process for Ge-surface cleaning following reference [3]. Prior to loading in the deposition chamber, samples were cleaned by holding it in highly concentrated HF vapor for 10 to 15 s. High-k TiO_2 and ZrO_2 films (~14 nm) were then deposited using metallorganic compounds titanium tetrakis isopropoxide [$Ti(OC_3H_7)_4$] and zirconium tetratert butoxide [$Zr(OC(CH_3)_3)_4$] in a microwave (700 W, 2.45 GHz) PECVD system at 500 mTorr for 1 min. No external biasing or heating of the substrate was employed; although the plasma discharge itself raised the substrate temperature to about 150 °C. For electrical measurements, metal insulator semiconductor (MIS) capacitors were

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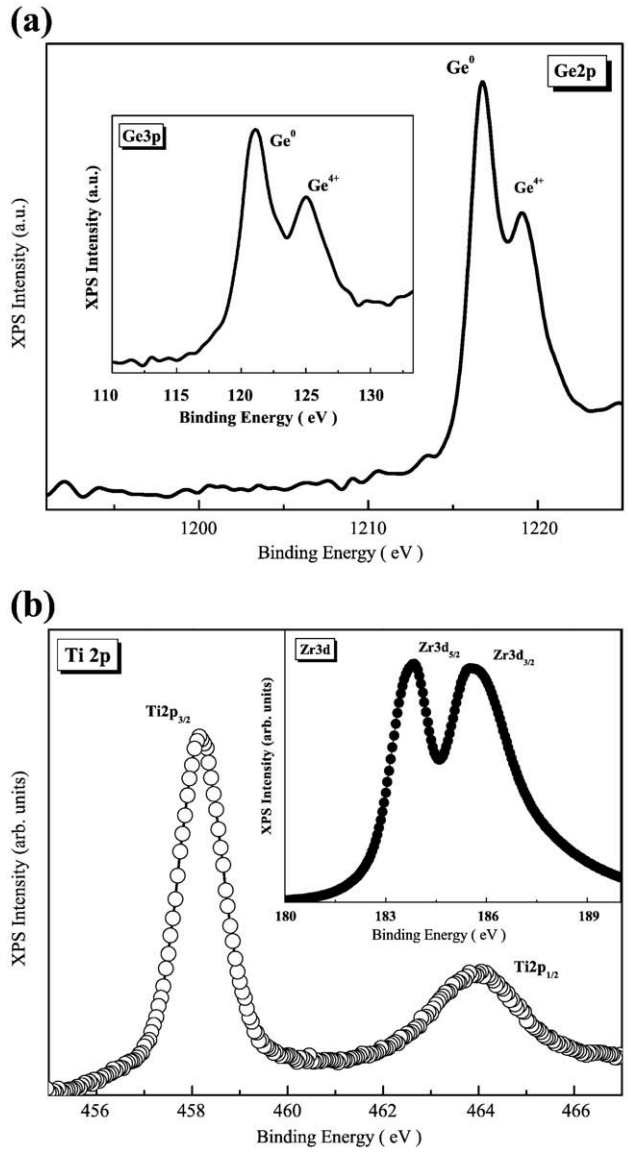

Fig. 1. High-resolution XPS spectra of (a) Ge 2p, Ge 3p (inset) and (b) Ti2p and Zr3d (inset) spectra of deposited TiO_2 and ZrO_2 films on Ge.

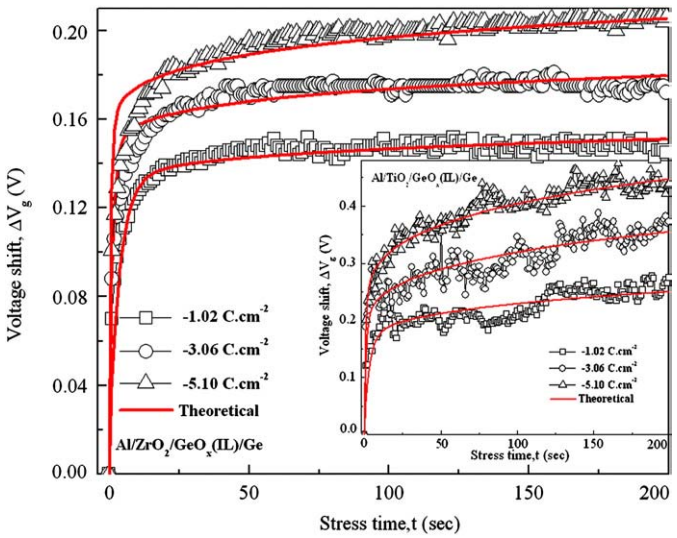

Fig. 2. Time dependent gate voltage shift (ΔV_g) during CCS for ZrO_2/GeO_x(IL)/Ge structure and TiO_2/GeO_x(IL)/Ge structure (inset).

fabricated by evaporating circular Al metal dots (area: 0.196 mm^2, thickness: 100–200 nm) through a shadow mask. Electrical characterization was done by HP 4145B and HP 4061A semiconductor parameter analyzer.

3. Result discussion

3.1. Chemical characterization

The high-resolution XPS measurement used for chemical composition analysis was performed under UHV condition (~2×10^{-9} mbar) using monochromatic Al K_α source (1486.7 eV) at room temperature. All data were recorded at 45° take-off angle that is in normal emission geometry. To get the composition of the stack layers the sputter profiling of the films was accomplished using an argon ion (Ar^+) beam with energy of 3 keV. The chamber pressure was kept at 1×10^{-6} mbar during sputtering. Fig. 1(a) shows the core-level spectra of Ge 2p and Ge 3p taken after etching. From XPS spectra both metallic Ge (Ge^0) peak at 1217.3 eV for 2p and 121.3 eV for 3p and fully oxidized state of

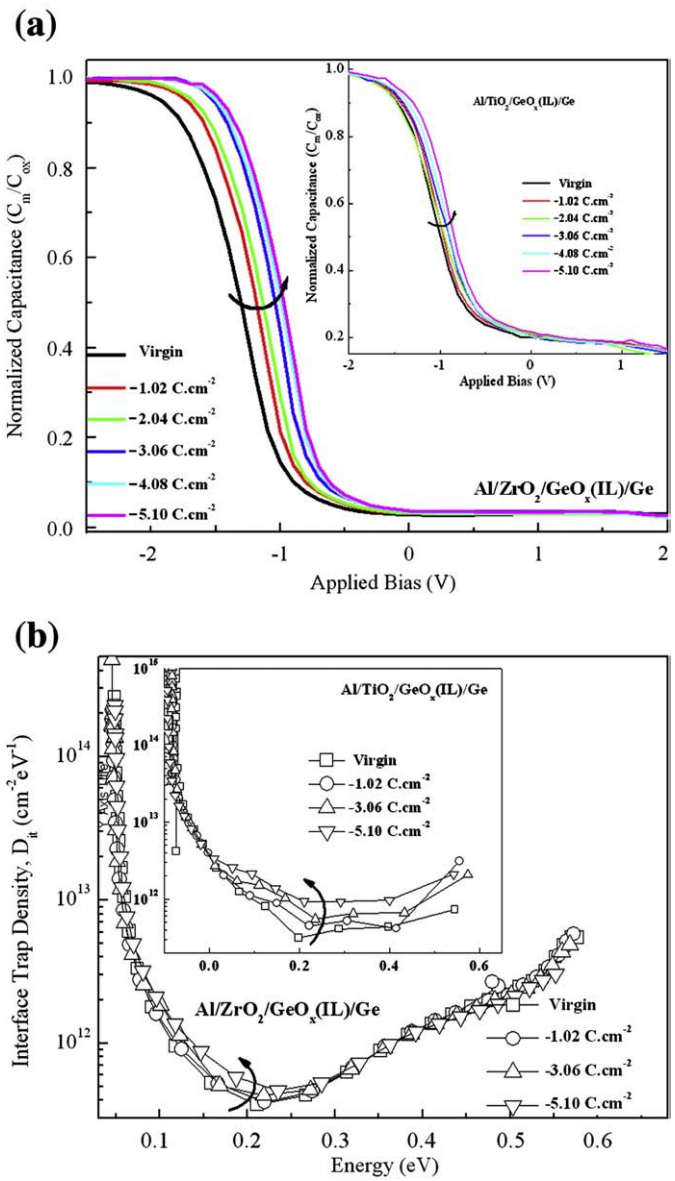

Fig. 3. (a) High frequency (400 kHz) normalized C–V characteristics ZrO_2/GeO_x(IL)/Ge structure and TiO_2/GeO_x(IL)/Ge MIS capacitors before and after stressing and (b) Energy distribution of density of interface states before and after stressing.