Comprehensive studies on the stabilities of a-In-Ga-Zn-O based thin film transistor by constant current stress

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ABSTRACT

Stability under constant current stress, along with hysteresis characteristics, was studied for a-In-Ga-Zn-O thin-film transistors (TFTs) in several atmospheres and at several temperatures. Unannealed TFTs showed rather large instability; i.e., large hysteresis in transfer curves ($\Delta V_G > 0.8$ V) and large positive threshold voltage shift ($\Delta V_{th} > 10$ V for 50 h tests at 5 µA) with deterioration of subthreshold voltage swing was observed. The instability for the unannealed TFT had a strong dependence on the stress atmosphere and the stress temperature, which suggests that trap states generated by the stress test is related to oxygen vacancy formed by breaking weak chemical bonds. Wet annealing improved stability; the hysteresis disappeared and the ΔV_{th} was reduced to <2 V. The improvement is considered to be related to the reduction of weak chemical bonds by wet annealing with the strong oxidation power of water molecules.

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1. Introduction

Transparent amorphous oxide semiconductors (TAOSs) such as a-In-Ga-Zn-O (a-IGZO) are expected for channel materials of thin-film transistors (TFTs) because they exhibit better TFT characteristics than those of hydrogenated amorphous silicon (a-Si:H) and organic TFTs; e.g. a field-effect mobility exceeds ~10 cm^2(Vs)$^{-1}$ and off current is easily suppressed to $<10^{-13}$ A even fabricated at room temperature (RT) with ohmic metal contacts [1–3]. Therefore, several applications to flat-panel displays and flexible devices such as active-matrix liquid-crystal displays (AMLCD), organic light-emitting diode displays (AM-OLED) and electronic papers (e-paper) have been demonstrated using a-IGZO-TFTs as a driving/switching TFT [4,5].

It is widely known that a post-thermal annealing is effective to improve not only TFT characteristics (i.e., mobility and small sub-threshold voltage swing (S)), but also their stability, which would originate from the reduction of subgap defect states in a-IGZO channel layer [6]. Recently, we have reported that wet O$_2$ annealing is more effective than dry O$_2$ annealing to improve TFT characteristics including their uniformity [7]. Therefore, most of the a-IGZO TFTs reported to date by companies are subjected to post-thermal annealing, and these exhibit good device characteristics such as a large mobility >10 cm^2(Vs)$^{-1}$, a small S value ~0.1 V/decade, and a large ON/OFF current ratio $>10^{10}$, which satisfy the requirements for practical high-resolution AM-OLED and large-size AMLCD. Several prototype displays such as 12.1″ AM-OLED and 15″ AMLCD have already been demonstrated using a-IGZO TFTs for driving TFTs [8,9].

To date, the focus of the development research is shifting to more practical issues such as stability and reliability of TFT characteristics. In particular, threshold voltage (V_{th}) stability under voltage/current stress is important for flat-panel display applications because driving current is changed by V_{th} shifts and consequently pixel signal level/emission intensity is altered [10]. Therefore, V_{th} stability against voltage/current stress for a-IGZO TFTs have been intensively studied [11–14]. Recently, we have found that the V_{th} shifts induced by constant current stress have multiple origins and large V_{th} shifts >10 V in unannealed a-IGZO TFTs are related to shallow subgap traps, which are annihilated by thermal annealing at 400 °C. Deep charged trap states remain even after the thermal annealing and cause small V_{th} shifts less than 2 V [15].

To further understand the origin of instability in a-IGZO TFTs under current stress, it is important to investigate the stability in a wide range of conditions such as different atmospheres and temperatures, because defects such as oxygen deficiency often cause electron trapping and doping in oxide semiconductors and their formation is sensitive to an atmosphere and temperature. In this work, we have investigated stability of a-IGZO (In:Ga:Zn = 1:1:1) TFT under constant current stress with several atmospheres and at different temperatures.

2. Experimental detail

2.1. TFT fabrication

All the a-IGZO (In:Ga:Zn = 1:1:1) films with thickness ~40 nm were deposited on thermal SiO$_2$ (t ~150 nm)/n$^+$-Si substrates by

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pulsed laser deposition with a KrF excimer laser ($\lambda = 248$ nm) at room temperature (RT). A sintered body of crystalline InGaZnO$_4$ was used as a target. Oxygen partial pressure during deposition was set to ~6.1–6.7 Pa. The a-IGZO channel regions were patterned by photolithography and lift-off. Then, thermal annealing was carried out at 400 °C for 1 h in dry or wet O$_2$ atmospheres (hereafter referred to as 'dry annealing' and 'wet annealing', respectively). The wet O$_2$ gas was generated through deionized water at 60 °C, which temperature corresponds to the H$_2$O partial pressure of 19.7% [7]. Then source/drain electrode areas were defined by photolithography, and a stacked layer of Au and Ti was deposited by electron-beam evaporation at RT. The channel width (W) and length (L) were 300 and 50 μm, respectively.

2.2. TFT characterization

TFT characteristics were measured by a semiconductor parameter analyzer at RT in dark. Saturation mobility (μ_{sat}) is extracted from $I_{DS} = W\mu_{sat}C_{OX}/2L(V_{GS} - V_{th})^2$, where I_{DS} is drain-source current, V_{GS} is gate-source voltage, and C_{OX} is the gate insulator capacitance per unit area; while a S value is evaluated using $S = (d\log I_{DS}/dV_{GS})^{-1} = 2.3k_BT/e$ $(1 + C_{sg}/C_{OX})$, where k_B denotes the Boltzmann constant, T the temperature, e the elementary electric charge and C_{sg} the equivalent capacitance contributed by the subgap states both in bulk and interfaces [16]. V_{th} is determined by extrapolating a straight line in a $(I_{DS})^{1/2} - V_{GS}$ plot to the V_{GS} axis. Constant current stress tests at a current of 5 μA, in which the drain electrode was connected to the gate electrode, were performed in air, dry O$_2$ and vacuum (~10^{-1} Pa) atmospheres at RT. The temperature dependences of constant current stress tests were also observed in the temperature range from 25 to 110 °C in air.

3. Result and discussions

3.1. Hysteresis characteristics and stability against ambient air

Fig. 1 shows typical transfer curves for the unannealed (a), dry annealed (b), and wet annealed (c) TFTs with the a-IGZO channels deposited at P$_{O2}$~6.7 Pa. The unannealed TFTs exhibit moderately good saturation mobilities (μ_{sat}) of ~7.2 cm^2(Vs)$^{-1}$, but the S value is somewhat large, ~0.42 V decade^{-1}, which suggests that high-density electron traps exist in the unannealed a-IGZO channel and/or interface. Correspondingly, the unannealed TFTs have a relatively large clockwise hysteresis in the transfer characteristics ΔV_G ~+0.8 V

(measured at a sweep rate of ~3 V/s), which is explained by trap filling by accumulated electrons. Thermal annealing improved not only TFT characteristics but also the hysteresis characteristics. For example, the dry annealed TFTs improved μ_{sat}, S and ΔV_G to ~9 cm^2 (Vs)$^{-1}$, ~0.18 V decade^{-1}, and ~+0.1 V, respectively. The wet annealed TFT exhibited further improved characteristics such as μ_{sat} ~12 cm^2(Vs)$^{-1}$, S ~0.11 V decade^{-1}, and ΔV_G ~0.0 V. These indicate that electron traps are reduced by the thermal annealing, and the wet annealing is more effective to reduce them than the dry annealing is.

Next, we examined the influences of ambient air on the TFT characteristics such as stability of V_{th}. Fig. 2 shows the transfer curves of the initial states and after keeping them in air for 1 month. All the TFTs exhibited negative V_{th} shift (ΔV_{th}). The ΔV_{th} values were as small as −0.06 V for the wet annealed TFT, while the unannealed and dry annealed TFTs exhibited large negative ΔV_{th} of ~−2.4 V and −1.3 V, respectively. It is in general known that the V_{th} is largely affected by several causes such as the donor density in a semiconductor channel, and the existence of charged states in a channel/interface region, and negative ΔV_{th} is explained both by the increase in donor density and the decrease in positively-charged states.

The transfer characteristics in the unannealed TFTs also showed large deterioration in the S value from ~0.52 to ~0.66 V decade^{-1} after 1 month (Fig. 2(a)), although μ_{sat} was nearly unchanged (~8.7 to ~8.9 cm^2(Vs)$^{-1}$). In contrast, both the dry and wet annealed TFTs exhibited no degradation in the TFT characteristic parameters after 1 month (from S ~0.23 V decade^{-1} and μ_{sat} ~8.6 cm^2(Vs)$^{-1}$ to ~0.22 V decade^{-1} and ~8.3 cm^2(Vs)$^{-1}$ for the dry annealed TFTs, from ~0.12 V decade^{-1} and ~11.7 cm^2(Vs)$^{-1}$ to ~0.12 V decade^{-1} and ~11.9 cm^2(Vs)$^{-1}$ for the wet annealed TFTs). The S value is very sensitive to subgap trap states around the Fermi level of a semiconductor channel and is deteriorated by increase in the subgap trap density [17]. Therefore, these results suggest that donor states and extra subgap trap states are formed for the unannealed TFTs even if simply placed in air at room temperature.

First-principles calculations showed that oxygen deficiency in a-IGZO plays important roles for both the electron doping and the formation of trap states, which depend on the local atomic configurations around an oxygen deficiency; i.e. an oxygen deficiency having a large free space forms both a deep occupied state and a shallow electron trap. While, if an oxygen deficiency does not have a large free space, it
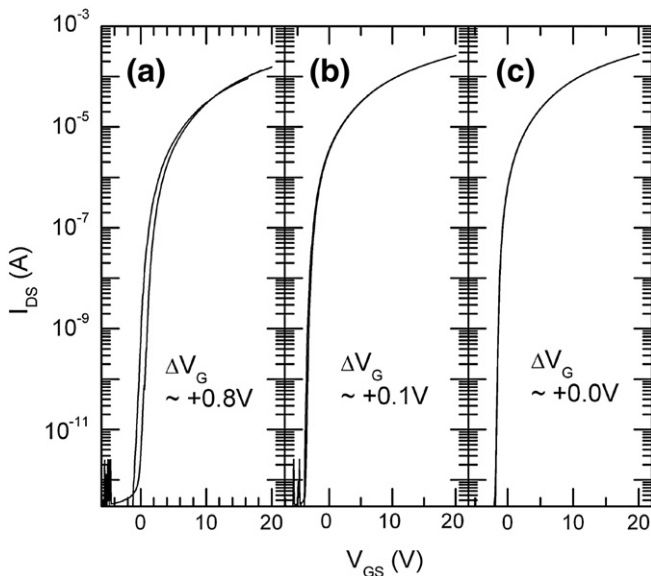

Fig. 1. Hysteresis in transfer characteristics at $V_{DS} = 10$ V for (a) unannealed, (b) dry annealed, and (c) wet annealed a-IGZO TFTs. The sweep rate was ~3 V/s.
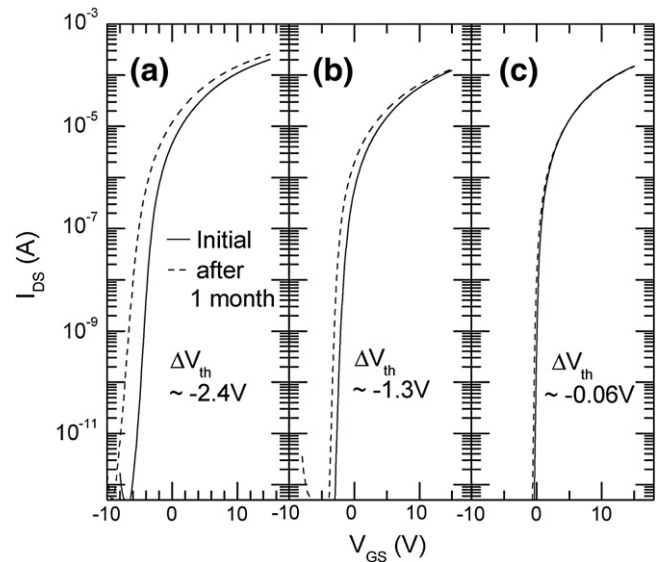

Fig. 2. Transfer characteristics of (a) unannealed, (b) dry and (c) wet annealed a-IGZO-TFTs at initial (solid lines) and after one month (dashed lines). The devices kept in air with 40–50% of humidity at RT. The unannealed a-IGZO channels were deposited at P$_{O2}$~6.1 Pa.