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Future challenges in CMOS process modeling

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ABSTRACT

Development and optimization of electronic devices in industrial and academic environments would hardly be conceivable without the numerical simulation of their processing and electronic behavior. In the past, model development efforts aimed especially at predicting junction depths. With the paradigm shift towards ultra-thin body silicon-on-insulator devices and FinFET architectures, the main emphasis changed to activation and lateral diffusion. Based on simulations of the electrical behavior of such advanced devices, the requirements on simulation of doping profiles will be explained. To achieve the high dopant activation needed to reduce contact and channel access resistances, active concentrations if possible above solid solubility are required. The concepts pursued involve annealing with low thermal budgets as well as defect engineering. A further paradigm shift concerns the semiconductor material used for future devices. While silicon, especially in a strained state, is still in the lead, research is also looking for alternative materials like germanium, germanium-rich silicon–germanium alloys, and III–V compounds. In order to be helpful, models for such processes and materials have to be provided as soon as possible even if the complexity of models for alternative materials lags behind contemporary models for silicon. The personal view of the authors is guided also by the International Technology Roadmap for Semiconductors for which one of us coordinates the modeling and simulation chapter.

1. Introduction

Predictions of future needs have usually a short lifetime when they concern the immediate future and remain necessarily vague when they address the remote future. For semiconductor devices, certainly the best guidelines are given by the International Technology Roadmap for Semiconductors (ITRS) which predicts and at the same time drives technological development. Because of its importance, it is described in more detail in Section 2. Future requirements on technology computer-aided design (TCAD) cannot only be found in the Modeling and Simulation Section of the ITRS. Within Europe, the industrial User Groups UPPER (User Group for Process Simulation European Research), UPPER + (User Group for Process Simulation European Research + Device Simulation) [1] and SUGERT (Strategic User Group for European Research on TCAD) [2] collected and published detailed and prioritized specifications to stimulate the required research activities. In comparison to the ITRS, the SUGERT specifications were significantly more detailed and meant to complement the ITRS. During its periods of operation, the European User Groups formed the European part of the International Technology Working Group (ITWG) of the Modeling and Simulation Section of the ITRS.

Due to the predicted changes in device architecture from bulk transistors to thin-body silicon-on-insulator or FinFET architectures, junction depth as one of the classical goals of junction engineering became significantly less important. In the TCAD chain, process simulation has to provide detailed information about topography and dopant distributions. Section 3 presents an investigation of the requirements of device simulation on the accuracy really needed for dopant profiles. The simulations make clear that the electrical activation of source/drain regions and the lateral doping profiles are particularly important to correctly predict the static and dynamic performance of devices.

To achieve especially the high dopant concentrations needed for the required high on-currents and low MOSFET delays, various technological options are pursued. They involve sophisticated annealing strategies, the co-implantation of impurities, defect engineering, and the application of strain. Section 4 summarizes the concepts and outlines the particular problems for predictive process modeling.

Mechanical stress is used as a technology booster to increase the charge carrier mobilities along specific crystallographic directions. But mechanical stress has not only a salient influence on mobility. It also influences the diffusion of intrinsic point defects and impurities as well as the formation of defects while defects and impurities vice versa influence the mechanical stress. Section 5 summarizes the effects that need to be considered for predictive process simulation.

Finally, since the physical limits for silicon are gradually approached, new materials are considered as technical options for

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future device channels. A typical material taken as example in Section 6 is germanium. Although research in germanium has gained considerable momentum again after decades during which the main concern of semiconductor research was silicon, it will need severe efforts to bring the predictability of process simulation close to that in silicon. This is even more true for other materials with high charge carrier mobilities such as III–V compounds.

2. CMOS process modeling in the ITRS

The International Technology Roadmap for Semiconductors ITRS [3] is the most important industrial strategy paper which specifies the research needed to continue the rapid development of semiconductor technology and devices towards higher performance and lower area and costs per function. Since 2000 it has extended the formerly US-based "National Technology Roadmap for Semiconductors" (NTRS) and strongly contributed to the continuation of the famous "Moore's law" [4], which already decades ago predicted an exponential development of almost all aspects of semiconductors. The ITRS is organized by the semiconductor associations of Europe, Japan, Korea, Taiwan and the USA. Representatives from leading semiconductor companies around the world agree on a common assessment about the timing of key features like DRAM half pitch, the physical gate length of a microprocessor unit or the chip frequency. Currently, sixteen so-called "International Technology Working Groups" ITWGs then derive from these target figures the necessary technologies and methodologies in all required areas of research, ranging from "System Drivers" and "Design" through topics like "Front-End Processes" and "Process Integration, Design and Structures" until "Factory Integration". Some of these ITWGs deal with crosscut techniques like "Metrology" or "Modeling and Simulation", which do not directly contribute to device fabrication but support all other areas of the ITRS. Having served as a yardstick for the technological development in the semiconductor industry, NTRS and ITRS have strongly contributed to the continuation of Moore's original scaling prediction, from less than 100 components per IC in 1965 to about 17 billion now in a current state-of-the-art DRAM chip.

"Modeling and Simulation" in the ITRS has a scope which extends beyond classical TCAD. Ranging from equipment impacts until circuits and packages, the modeling subchapters include equipment/feature scale, lithography, front-end process, device, interconnects and integrated passives, circuit elements modeling, and finally package simulation. Additionally, three subchapters deal with enabling techniques which are required by or influence all these seven areas: Materials modeling, numerical methods, and finally TCAD for design, manufacturing and yield. One of the key messages given in the Modeling and Simulation chapter of the ITRS is that the potential for the reduction of technology development costs was estimated at 40% in the 2007 ITRS.

One of the six short-term difficult challenges for Modeling and Simulation is "Front-end process modeling for nanometer structures" which largely deals with various aspects of dopant diffusion and activation. For the fabrication of current aggressively scaled devices, sophisticated ultra-short time annealing processes are employed. Stress is on one hand side intentionally introduced to increase carrier mobility, on the other hand side unintentionally created e.g. by inhomogeneous temperature distributions. Alternative channel materials are another option to increase carrier mobility and, in turn, circuit speed. Advanced device architectures are no more an option but a must to further continue scaling. Because in real technology most of these effects usually show up in parallel and impact on each other, they must also be simultaneously described by state-of-the-art physical models. This led to a first and rather complicated request in the challenge on "Front-end process modeling for nanometer structures", namely "Coupled diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe:C, Ge, GaAs, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers." Therein, the acronyms SPER and SOI stand for "Solid-Phase Epitaxial Regrowth" and "Silicon-On-Insulator", respectively. The next two requirements of this challenge complement this first one: "Modeling of epitaxially grown layers: Shape, morphology, stress", and "Modeling of stress memorization (SMT) during process sequences". The need for on one hand side accurate and predictive simulation, on the other hand side acceptable memory and computation time results in the next requirement: "Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces". The need for appropriate experimental evaluation of the models developed leads to the requirement "Characterization tools/methodologies for ultra shallow geometries/junctions, 2D low dopant level, and stress". Moreover, in order to enable the simulation of industrially relevant advanced device architectures, "Efficient and robust 3D meshing for moving boundaries" are required. The final requirement of this challenge, "Front-end processing impact on reliability", already bridges to the short-term challenge on "Ultimate nanoscale device simulation capability".

3. Requirements from device simulation

As a baseline for the challenges coming along with future CMOS device architectures, device simulations of fully-depleted silicon-on-insulator (FD SOI) nMOS and pMOS transistors were performed. The major aim of this simulation study was to illustrate the accuracy to which dopant profiles have to be known via their effects on the electrical performance of this MOSFET architecture. For demonstration, the low standby power (LSTP) specifications of the 32 nm technology node were used with specifications taken from the ITRS.

The SentaurusStructureEditor of Synopsys [5] was used for creating the MOSFET structures. As specified by the ITRS, a physical gate length L_{gate} of 20 nm and an equivalent gate oxide thickness t_{ox} of 1.2 nm were used. The length of the source and drain contacts was set to four times the gate length (80 nm). The thickness of the silicon body t_{body} was set to 5 nm, which is a fourth of the physical gate length, while a thickness of 10 nm was used for the buried oxide (BOX). Additionally, an elevation of the source and drain regions by a selective epitaxial growth (SEG) of a 20 nm layer was assumed. Finally, a heavy ground plane doping [6] below the buried oxide of 1×10^{20} cm^{-3} of boron and arsenic for nMOS and pMOS transistors, respectively, was used to suppress short-channel effects. The channels were kept undoped, as it is usual for this kind of MOSFET architectures. The geometrical shape is displayed in Fig. 1 with the doping shown for the case of the nMOS device.

Device simulations were performed using SentaurusDevice of Synopsys [5]. They were based on the drift-diffusion approximation employing several standard models for carrier generation–recombination [7], carrier mobility impact by impurities [8], surface roughness

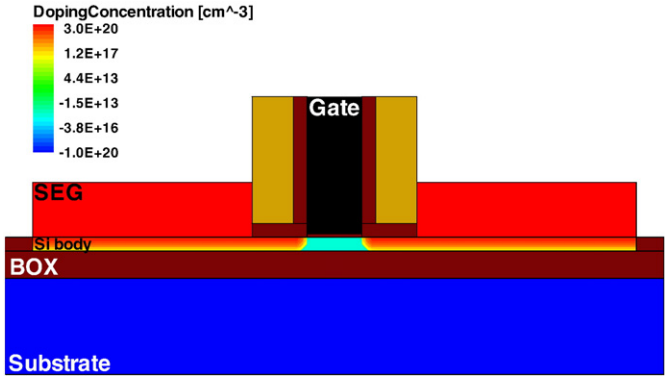

Fig. 1. MOSFET architecture used in the device simulation study. The doping is shown for the nMOS device.