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Deep level transient spectroscopy study for the development of ion-implanted silicon field-effect transistors for spin-dependent transport

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ABSTRACT

A deep level transient spectroscopy (DLTS) study of defects created by low-fluence, low-energy ion implantation for development of ion-implanted silicon field-effect transistors for spin-dependent transport experiments is presented. Standard annealing strategies are considered to activate the implanted dopants and repair the implantation damage in test metal-oxide-semiconductor (MOS) capacitors. Fixed oxide charge, interface trapped charge and the role of minority carriers in DLTS are investigated. A furnace anneal at 950 °C was found to activate the dopants but did not repair the implantation damage as efficiently as a 1000 °C rapid thermal anneal. No evidence of bulk traps was observed after either of these anneals. The ion-implanted spin-dependent transport device is shown to have expected characteristics using the processing strategy determined in this study.

1. Introduction

Solid-state quantum computers require spin readout and control in order to transfer information to and from spin-encoded electrons or nuclei. A number of readout pathways have been identified based on spin-to-charge conversion [1,2]. Recently, spin-dependent transport properties in a bulk-doped field-effect transistor (FET) observed by electrically detected magnetic resonance (EDMR) has been demonstrated and is therefore also a candidate for spin readout and control [3]. In this work, a broadband on-chip terminated stripline is used to perform electron spin resonance on the hyperfine states of phosphorous donors in a silicon MOSFET (bulk doped). A second generation version of this device utilizing ion implantation technology may refine the MOSFET properties through the precision control of the depth, concentration and type of implanted dopants.

Ion implantation is widely used in the fabrication of semiconductor devices. Spatial control is also easily achieved through the use of masks. High-quality oxide growth after implantation is problematic as implanted dopants will diffuse unless a dopant with a low diffusion coefficient is chosen such as Sb [4,5]. Alternatively, a low temperature high-quality oxide growth may be performed after implantation to avoid any significant dopant diffusion [6]. In another approach, implantation can be performed through the oxide itself. Recently, implantation through a 5 nm oxide layer followed by a rapid thermal anneal (RTA) was shown not to increase the SiO_2/Si interface trap density and was in fact found to be beneficial when the as-grown oxide interface trap density is abnormally high [7].

Deep level transient spectroscopy (DLTS) is well-suited to quantify the low defect concentrations that can still be detrimental to device operation. In this work, measurements are presented for ion-implanted MOS capacitors used to optimize the processing strategy of spin-dependent transport FETs. As implantation is used as any spurious signals arising from microwave absorption of the P donors in the bulk and in the P-diffused source and drain contacts in these FETs are avoided. The activation of donors as well as the minimization of oxide and interface traps are investigated.

2. Experiment

Substrates for the test MOS capacitors were n-type, P-doped Si (100) Czochralski-grown wafers with a resistivity of 5–10 Ω cm. The FETs described above were fabricated on an n-type, P-doped Si^{28} (100) epilayer with a resistivity of 110 Ω cm. Initially, a 200–300 nm thick uniform field oxide was thermally grown on both wafers in a wet O_2 ambient. Phosphorous in-diffusion in photolithographically etched back regions was then used to form the source and drain of the FET. A central window in the channel region of the FET and circular regions in the test wafer were etched back for growth of a 20 nm high-quality oxide grown using a triple wall furnace at 800 °C in a dry O_2 ambient. Dichloroethylene (DCE) was introduced during the growth to prevent ionic impurities being incorporated.

Fig. 1 shows a simulation using SRIM [8] of the 30 keV As implant profile performed into the channel region of the FET and the circular regions of the test capacitors to a fluence of $2\times10^{11}\,cm^{-2}$. This implant gives a peak concentration of $0.9\times10^{17}\,As/cm^3$ at a depth of

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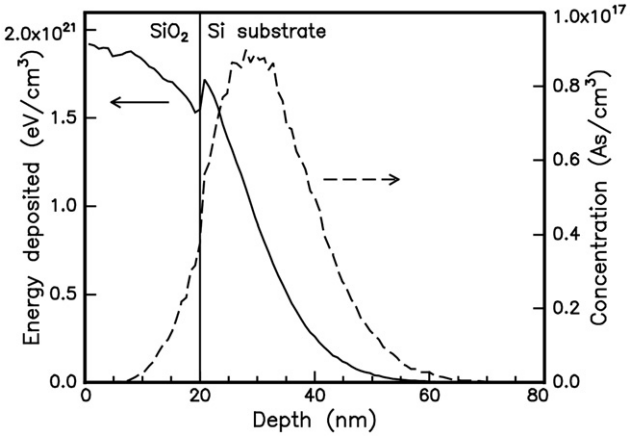

Fig. 1. Energy deposited and concentration profile simulation of 30 keV As to a fluence of $2\times10^{11}\,cm^{-2}$ using SRIM [8]. The Si/SiO_2 interface is indicated by the vertical line.

10 nm beyond the Si/SiO_2 interface, corresponding to an As donor spacing of about 20 nm. This is similar to the P spacing in the proposed solid-state quantum computer [9]. Most of the energy of the implant is deposited into the oxide. To repair the damage and activate the dopants various standard annealing strategies were considered. A rapid thermal anneal (RTA) at 1000 °C for 5 s in a nitrogen ambient, a 950 °C, 30 min furnace anneal (FA) in a forming gas ambient (95% N_2, 5% H_2) and a combination of RTA and FA (RTA + FA) were used. The diffusion length ($\sqrt{4D_{As}t}$) of the implanted As determined by the As diffusion coefficient, D_{As}, was found to be 1.8 nm and 16.3 nm for these RTA and FA anneals, respectively [10].

After the anneal, each sample underwent a passivation anneal in forming gas for 15 min at 400 °C. This anneal reduces the interface trap density by 20%. Al was then evaporated to form the gate and ohmic contacts over the source and drain. The circular regions of the test wafer and the entire back surface were metallized with Al. Following metallization a further forming gas anneal was performed.

Capacitance voltage (CV) and deep level transient spectroscopy (DLTS) were performed with a SULA Technologies DLTS system to characterize the MOS capacitors in a temperature range 80–370 K. The interface trap density was determined using the methodology outlined by Johnson and a capture cross section of $5\times10^{-15}\,cm^2$ was assumed [11].

3. Results and discussion

Fig. 2 shows the CV obtained from the MOS capacitors having undergone the three different annealing strategies. The CV from a control sample that had no implantation or high temperature anneal is shown for comparison. Samples that had undergone an RTA at some stage had similar CV profiles. The FA sample was shifted further to negative voltages and had a slightly higher inversion capacitance. All CV curves show a weak inversion response which is due to interface traps [12,13]. The presence of an activated As profile near the Si/SiO_2 interface will also increase the capacitance in weak inversion. In addition, the active donors will shift the flat-band voltage since the metal–semiconductor work-function difference will vary with shifts in the Fermi level in the semiconductor. Likewise, fixed oxide charge deposited into the oxide by implantation also shifts the flat-band voltage down. To qualitatively de-convolute these contributions we simulated the CV profiles using TCAD [14] as shown in the inset of Fig. 2. No defects in the oxide or at the Si/SiO_2 interface were included in these simulations so that only changes due to the As implant could be observed. The simulation shows that the implantation does not shift the curve to lower voltages by any appreciable amount. Therefore, a large component of the shift in these experimental CV curves is attributed to fixed oxide charge. Although the FA is most efficient at activating the dopants indicated by the increase in the inversion capacitance, a comparatively large amount of fixed oxide charge remains after the anneal. The fixed oxide charge is estimated to increase by $2.9\times10^{11}/cm^2$ whereas the RTA sample results in an increase of $1.6\times10^{11}/cm^2$. This is calculated assuming that the shift is entirely due to the fixed oxide charge and therefore represents an upper limit.

Fig. 3 shows the DLTS correlator signals as a function of temperature. A continuous background as well as a large peak near room temperature is observed in all samples. These peaks are associated with minority carrier generation–recombination processes [15,16]. These will be discussed further below. No peaks associated with bulk traps produced by the implantation were observed after any of the anneals. The interface trap density, D_{it}, calculated from the low temperature part of the spectra where emission from majority carriers dominates was $1.4\times10^{10}/eV/cm^2$ for the control sample. The RTA and (RTA + FA) both retained a low D_{it} of $1.3\times10^{10}/eV/cm^2$. The FA had a slightly higher D_{it} of $1.9\times10^{10}/eV/cm^2$. These values are the densities of interface traps in the band gap at an energy of $(E_c - E_t) = 0.16$ eV.

The large peaks in Fig. 3 are due to generation–recombination processes through interface minority carrier traps near the centre of the band gap. The activation energy and capture cross section of this process can be determined using an Arrhenius plot of e_p/T^2 versus $1/kT$ according to the hole emission rate equation [17]

$$e_p = \sigma_p v_{th} N_V \exp\left(\frac{E_f - E_V}{kT}\right) = \sigma_p \gamma_p T^2 \exp\left(\frac{\Delta E_h}{kT}\right) \quad (1)$$

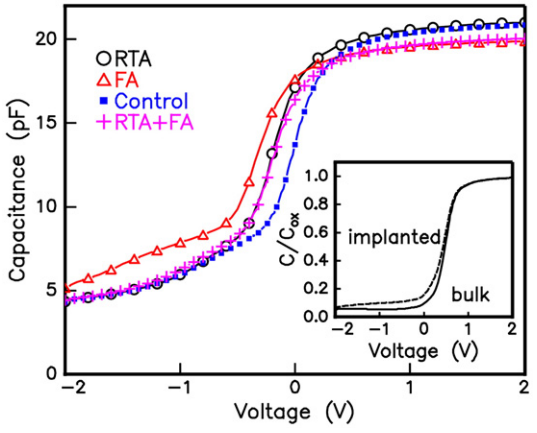

Fig. 2. Capacitance–voltage curves of processed MOS test capacitors measured with an AC frequency of 1 MHz. The measurement temperature was 300 K. The inset shows the simulated CV of a bulk doped (solid line) and As implanted wafer (dashed line).

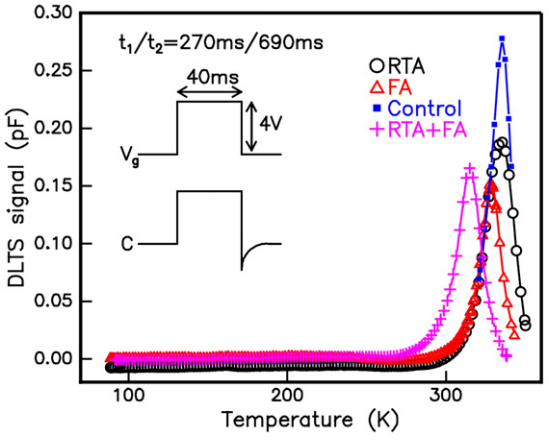

Fig. 3. DLTS signal as a function of temperature with the correlator time window defined by $t_1 = 270$ ms and $t_2 = 290$ ms. The voltage pulse (from −2 V to 2 V) and corresponding capacitance transient is also shown.