



Influence of the epitaxial growth and device processing on the overlay accuracy during processing of the d-DotFET

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ABSTRACT

To maintain the development of MOSFET devices in the last three decades the lateral layout of this important device was scaled down into the sub-50 nm range. The challenge to maintain device performance was met by applying to scaling rules, which ensure a proper physical behaviour in the active area of the device. But nowadays new device architectures as Ultra Thin Body and Multi Gate devices have to be discussed. Furthermore new materials were introduced as high- κ gate dielectrics and metal gates. In recent years strained silicon has drawn increasing attention to enlarge carrier mobility in the MOSFET channel. In the d-DotFET approach locally strained silicon is formed by means of template-assisted self assembly of Ge-dots and silicon overgrowth. The silicon capping layer is strained on top of the dot and in its near vicinity, only. The accurate positioning of the dots on pre-patterned substrates enables the utilization of these substrates for further device processing. The crucial issue is to integrate the active area on top of the dot, which requires an overlay of ± 10 nm, which has to be assured over the whole process. In this paper we investigate the intrinsic overlay of a Vistec EBPG 5000^{plus} e-beam system using etched holes in silicon as markers. It was found, that the required overlay accuracy can be obtained, when the definition of the marker sites is adapted to the following process, already. The overlay is not affected by device processing, as long as the markers are affected symmetrically.

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1. Introduction

The improvement of metal-insulator semiconductor field-effect transistor (MOSFET) devices facilitated the progress in microelectronics in the last decades. The scaled device dimensions gave rise to faster, denser and hence cheaper integrated circuits. This tremendous development is based on a top-down approach that exploits the MOSFET scaling rules, pushing the existing devices to their fundamental physical and reliability limits. In the first years of this evolution short channel effects were avoided by modifications of layout (S/D-extensions, halo-implantation etc.), but with shrinking device dimensions, the challenges to maintain device performance increase steadily. Therefore in recent years new layouts and materials (multiple-gate-structures, high- κ) had to be considered. Nowadays the replacement of the channel forming silicon by strained silicon is discussed. Straining silicon from its natural lattice constant changes the electronic band structure, which increases the carrier mobility, and hence the on-current of the MOSFET.

There were several approaches to utilize strained silicon for MOSFET applications. The most straight forward way is to grow silicon epitaxially on top of relaxed SiGe buffers; here the strain in the silicon

can be adjusted by the Ge content of the buffer layer. To utilize such materials for microelectronic applications it is important to achieve a low defect density at the surface. Growing thick layers with varying Ge fraction (graded buffer) is one widely used method for getting high quality relaxed SiGe surfaces [1]. Another approach [2,3] uses a thin (~200 nm) SiGe layer grown pseudomorphically strained on Si (100) substrates. By He implantation a high density of dislocation sources is induced into the substrate, which enables the efficient strain relaxation in the SiGe layer and a low dislocation density at the surface.

In contrast to the cited methods, by which homogeneously strained layers are fabricated, locally strained silicon can be obtained by template-assisted self organized growth of Ge-dots [4,5]. Hereby two facts are exploited: First, due to the large lattice mismatch, Ge will grow in Stranski–Krastanov-mode on silicon wafers. Second, the template-assisted self organisation: Here the sites, where the Ge-dot should grow are predefined by a patterning of the substrate. The resulting dots have a relaxed SiGe surface, where the Ge content depends on growth conditions. The epitaxially grown 20 nm thick silicon capping layer will be strained only on top and in the near vicinity of the dots. Due to the accuracy of the predefined dot sites, the integration of the MOSFET on the dots is possible and opens the advantages of locally strained silicon to the device.

For satisfying device behaviour it is indispensable to place the active area of the transistor on the dot. Therefore high resolution and

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high overlay accuracy lithography have to be used to obtain spatial accuracy of ± 10 nm. While for industrial production advanced optical lithography is used meeting the requirements of the proposed device [7] here, in research e-beam lithography is the method of choice for high resolution and high overlay accuracy lithography. Therefore in [6] the transistor process for this so called d-DotFET device is proposed using e-beam lithography for the sub-100 nm high overlay accuracy patterning. In this paper we investigate the intrinsic overlay obtainable with the Vistec EBPG 5000^{plus} e-beam lithography system and the influence of device processing.

2. Experimental

The Vistec EBPG 5000^{plus} is an e-beam lithography system for high level application. The sample is placed on a wafer stage, the position of which is measured by a laser interferometer (0.618 nm accuracy). The e-beam is extracted from an e-beam source and focused by an electron optical system. Before exposure, markers on the sample holder and the sample are measured to attach the sample to the coordinate system of the tool. For e-beam direct write the positions of three markers are measured and compared with their expected positions. From this comparison a correction of the coordinate system is calculated. The e-beam system can address a certain area without table movement, the so called mainfield. The size of the mainfield depends on the used grid dimension—the so called beam step size (bss). In this work a mainfield size of 500 μm was chosen.

Crucial for an accurate positioning on the wafer are the markers. Because high contrast metal pads are forbidden for Si-MOSFET applications, square holes in the silicon with vertical side walls, an edge length of 10 μm and a depth of 600 nm are used. Their positions are recognized by the drop of the intensity of the back scattered electrons at the rim of the marker. When the e-beam is scanned across the marker edge, the intensity signal is interpreted, giving the edge position. For each edge, this measurement is repeated 20 times along the edge, so the position and the standard deviation are determined. The centre of the marker is the middle of the two opposing edges in x- and y-direction, respectively.

The markers are defined by optical lithography and etched 600 nm deep into the silicon by reactive ion etching. The optical masks are written by e-beam lithography, too. In this work, two different markers layouts are used. In both cases 6 times 5 cells are defined. In each cell there is a marker in the lower left corner (bullets in Fig. 1); the three markers needed for adjustment in cell(x,y) are in cell(x,y), cell(x+1,y) and cell(x,y+1). In the first marker layout, in the centre

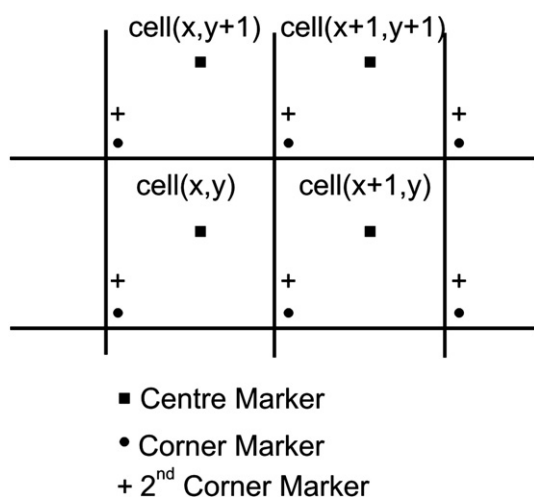


Fig. 1. Schematic view of the cell layout: squares represent the centre marker, circles the corner markers, which are used for measurement. For layout 2 “+” represents the marker set to define the position of the centre marker.

of each cell an additional marker (squares in Fig. 1) is defined on the same optical mask with the corner markers; furthermore, as usually done in mask production, the mainfield boundaries during mask writing were not adapted to the cell size. In the second layout, the mainfields during mask definition are adapted to the cells. Furthermore in the lower left corner of each cell a second marker is defined (“+” in Fig. 1) in the same mainfield. In contrast to layout 1, here the second marker set is used to define the centre marker in an additional e-beam lithography step.

Thus prepared samples were loaded into the e-beam system and the calibration process for the beam was performed. Afterwards for every cell the corner markers and centre marker in the cell itself (cell(x,y)), in the upper cell (cell(x,y+1)), in the upper right cell (cell(x+1,y+1)) and in the right cell (cell(x+1,y)) were measured 25 times; their positions and the standard deviations of the measurements of the marker edges were logged.

3. Results and discussion

For positioning it is important to measure distances very precisely. Therefore the standard deviation of the measurement of marker distances was evaluated. In Figs. 2 and 3 the standard deviations are plotted versus the beam current (Fig. 2) and the pattern resolution (Fig. 3). 120 different distances (30 cells, 4 distances in a cell) were measured 25 times. The filled squares show the errors calculated from the standard deviations of the single edge measurement applying the law of error propagation. The open circles represent the mean value of the standard deviations of the 120 distances measured 25 times. It can be seen, that the error is independent of the beam current for both analysis procedures (Fig. 2). Note that the resolution was held constant at 2.5 nm. The dependency on the resolution is unequal. While for applying the law of error propagation the error increases with lowering the resolution, for the normal statistical analysis the error is independent. The beam current was kept at 1 nA. The accuracy, with which the distance between markers can be measured, is better than expected from error propagation. This can be attributed to a curvature of the marker edge, which is symmetrical to the marker centre. Hence distances can be measured with accuracy better than 5 nm.

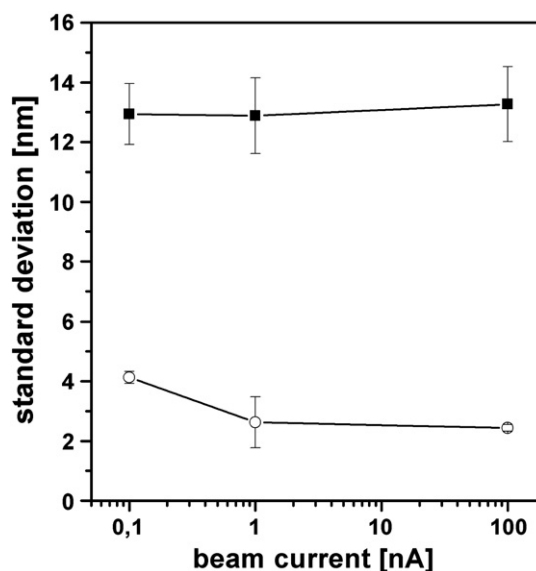


Fig. 2. Standard deviation of the distance between two markers calculated from the results of 25 measurements (○) and from the measured standard deviations of the single marker edge measurements applying the law of error propagation (■) versus beam current at constant resolution of 2.5 nm.

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