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Substrate current enhancement in 65 nm metal-oxide-silicon field-effect transistor under external mechanical stress

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ABSTRACT

An approach to get uniaxial tensile stress from the channel by using strained silicon to enhance drain current and mobility was developed. A 65 nm metal-oxide-semiconductor field-effect transistor (MOSFET) was bent by applying external mechanical stress. The drain current and transconductance of the transistor were found to increase 15% and 20%, respectively. In this paper, the behaviors of the substrate current and the impact ionization rate are also investigated. It was found that the substrate current and gate voltage corresponding to the maximum impact ionization current have significantly increased by increasing external mechanical stress. According to the relationship to the strain-induced mobility enhancement, the increase in impact ionization efficiency resulted from the decrease in threshold energy for impact ionization which was due to the narrowing of the bandgap.

1. Introduction

The size of integrated circuits technology has already been miniaturized to the nano-meter scale, which has improved performance and circuit density. However, for the constant off current limit, saturation drain current does not increase as size decreases. A strained-Si metal-oxide-semiconductor field-effect transistor (MOSFET) was recently developed for advanced high-performance and low-power complementary metal-oxide-semiconductor (CMOS), because of the enhanced electron and hole mobility resulting from modification of the band structure [1–4]. The strained silicon device can be fabricated by numerous techniques. A conventional approach in which biaxial strain was applied to the channel from the bottom using strained-Si on relaxed $Si_{1-x}Ge_x$ [5,6]. Since biaxial tensile stress generates advantageous strain for both n-type and p-type MOSFETs, it has potential technological importance to CMOS logic technologies. However, it has not been utilized to fabricate commercial CMOS microprocessors due to integration challenges, process complexity and cost. Additionally, most p-type MOSFETs under biaxial stress have near-zero hole mobility enhancement in large vertical electrical fields [3] in which commercial MOSFETs operate. To solve these problems, a technique was proposed that generated longitudinal uniaxial stress in both n- and p-type MOSFETs [7]. In p-type MOSFETs, a selective epitaxial $Si_{1-x}Ge_x$ in the source/drain regions was employed to create longitudinal uniaxial compressive strain, whereas n-type MOSFETs had a Si nitride-capping layer that introduced tensile uniaxial strain in the channel. Unlike previous work investigating strained-Si, this technique can control the amount of strain in n- and p-type MOSFETs independently on the same wafer, and enhance hole mobility in a large vertical electrical field. A similar method used Si_3N_4 to produce heavy mechanical stress and for Ge-ion implantation to selectively relax the stress in the layer [8]. It can also control the strain in n- and p-type MOSFETs independently. As gate length decreased, drive current and mobility were typically affected due to stress from shallow trench isolation [9]. The stress created by these techniques can be called intrinsic strain.

Conversely, the uniaxial compressive or tensile strain can be created by external mechanical stress, such as the four-point bending technique [10,11]. Although four-point bending is a simple technique, the stress applied on a wafer is non-uniform as stress is concentrate on the point. Furthermore, the device can not be placed on a thermal chuck, and thus, the temperature-dependent characteristics can not be analyzed. This work presents uniform bending method that efficiently improves drive current and transconductance. The silicon substrate was initially thinned by a polisher, and fixed on a holder with a specific curvature radius. A uniaxial strain can be generated in the channel using the proposed technique. In this work, tensile strain was created in the channel via the bending method.

Additionally, another concern for advanced CMOS is impact ionization phenomena caused by hot-carrier generated in high lateral

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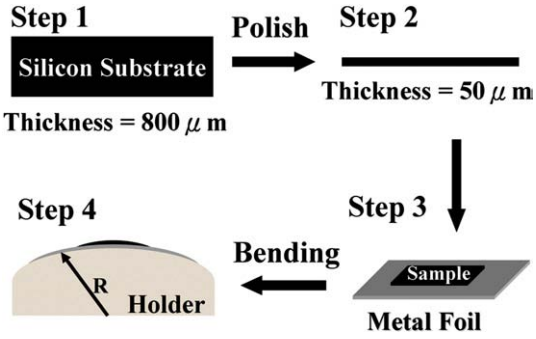

Fig. 1. The process steps of bending silicon substrate.

electrical field, which is associated with reliability problems in sub-100 nm MOSFETs. Therefore, the substrate current is a powerful parameter for predicting hot-carrier-induced degradation and lifetime in MOSFETs [12]. Strain-induced enhancement of impact ionization efficiency (IIE) has been widely investigated both uniaxial and biaxial stress [13,14]. In general, IIE depends on the carrier transport properties and the band structure. The effects caused by strain are as follows: 1) increased mobility (reduced inert-valley scattering); and, 2) narrowed bandgap energy (reduction of threshold energy for impact ionization). These two effects enhance IIE. The second effect was demonstrated to be a major factor in enhancing IIE [15]. In this work, the same phenomena were observed. Our interpretations of strain-induced substrate current enhancement are based on the aforementioned theory.

2. Experimental

Devices used in this work were n-MOSFETs with channel length of 65-nm and channel width of 10 μm, fabricated by a commercial 65 nm process on an industrial standard 12 inch Si wafers which the channel direction are parallel to Si <100>. The devices were patterned with 193 nm lithography. And the process flows are described as follow. The standard processes of shallow trench isolation, gate oxide, Si_3N_4 spacer, source/drain (S/D) implant, spike anneal, Ni salicide, and Cu interconnect processes were applied. Gate oxynitride thickness was 1.2 nm and gate polysilicon thickness was 98.5 nm, respectively. And an oxide-nitride-oxide (ONO) structure was used to form sidewall spacer. The preparation of bending device is described as follow; the thickness of silicon substrate was reduced from 800 μm to 50 μm by using Struers RotoPol-21 polisher. Subsequently, the silicon substrate was adhered to the metal foil by using adhesive tape which is heat-proof below 573 K. Finally, the metal foil was fixed on a bending holder with specific curvature radius. Therefore, the stress applied on the sample is uniform. Then, the mechanical stress was applied in parallel direction to the n-MOSFETs current flow. The measurement instrument was used Agilent 4156C. Device characteristics were measured at room temperature by imposing external mechanical stress along longitudinal direction. Hot-carrier effect study was carried out at a series steps V_D = 1.5 V, 1.6 V, 1.7 V, 1.8 V, and variable V_{GS}. The bending process steps are shown in Fig. 1 and the bending sample with radius 30 mm and 50 mm is illustrated in Fig. 2, respectively.

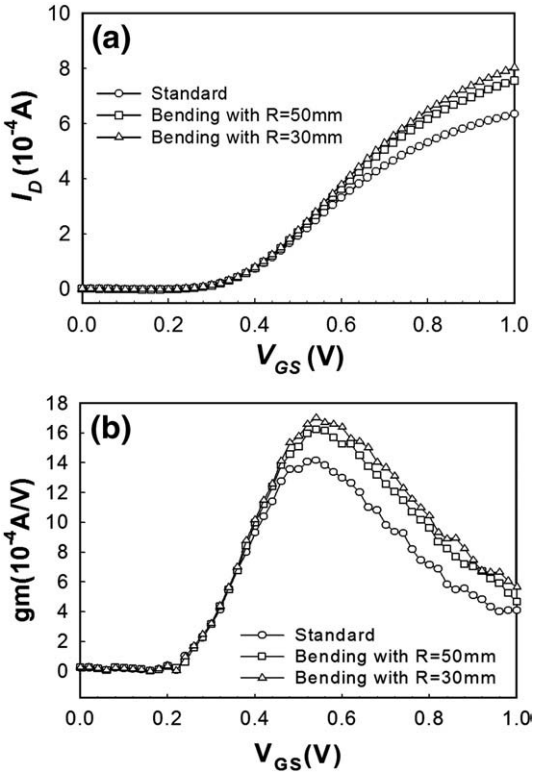

Fig. 3. (a) Drain current and (b) transconductance of standard and strained (R=30 and 50 mm) n-MOSFETs.

3. Results and discussion

The sample was bent via external mechanical stress applied along the channel length direction (Fig. 2), and a tensile strain was created in the channel. Fig. 3 presents the linear drain current (I_D) and transconductance

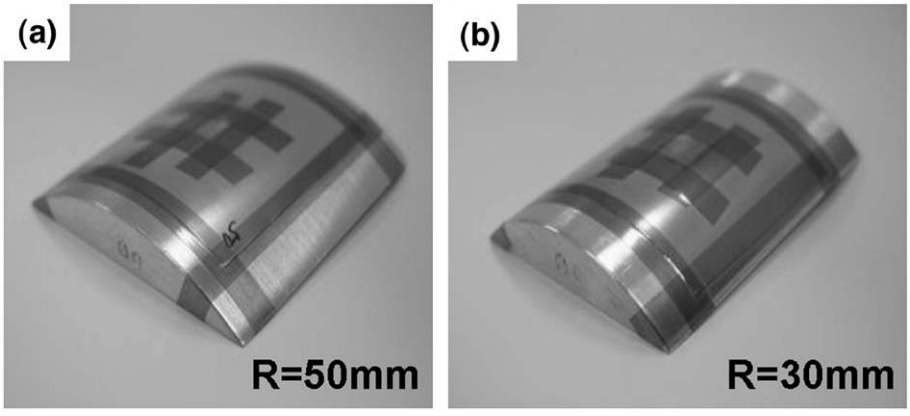

Fig. 2. Illustrations of samples bend on holders with curvature radius (a) R=50 mm and (b) R=30 mm.