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Letter

Fabrication of n-type Schottky barrier thin-film transistor with channel length and width of 0.1 μm and erbium silicide source/drain

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ABSTRACT

In this paper, a Schottky barrier polycrystalline silicon thin-film transistor (SB TFT) with erbium silicide source/drain is demonstrated using low temperature processes. A low temperature oxide is used for a gate dielectric and the transistor channel is crystallized by a metal-induced lateral crystallization process. An n-type SB TFT shows a normal electrical performance with subthreshold slope of 239 mV/dec, I_{ON}/I_{OFF} ratio of 5.8×10^4 and I_{ON} of 2 μA/μm at $V_G=3$ V, $V_D=2.5$ V for 0.1 μm device. A process temperature is maintained at less than 600 °C throughout the whole processes. The SB TFT is expected to be a promising candidate for a next system-on-glass technology and an alternative 3D integration technology.

1. Introduction

A low temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) is key devices in liquid crystal display and organic light emitting display technology [1,2]. LTPS TFTs are used in integrating pixel driving ICs on a glass panel for small and thin display applications. In LTPS TFTs, an issue is to lower the temperature of thermal process like channel crystallization and source/drain activation in order to integrate devices directly on a glass panel. The excimer laser annealing which is mostly used in a mass production has disadvantage that equipment and process cost are expensive and throughput is low [3,4]. LTPS TFT is suitable for 3D integration technology for evolution of system integration and multi-functional system-on-a-chip. In 3D integration, stacking known good die or wafer with through-silicon-via adoption is still expensive and challenging process [5,6]. However sequential stacking of polycrystalline TFT layers is simple and costs less [7,8]. The high quality crystallized poly-Si channel and gate dielectric with low temperature process become main issues for 3D integrated circuits with vertical stacked structure of poly-Si TFTs, because the lower devices and interlayer interconnection lines will be degraded by high temperature process during the fabrication of the upper devices. Recently Schottky barrier metal-oxide-silicon field-effect transistors (SB MOSFETs) fabricated by simple process at low temperature have been proposed as alternative to conventional MOSFETs [9–13]. In SB MOSFETs source and drain regions are composed of silicide instead of impurity doped silicon. Therefore SB TFT is expected to be one of the alternatives for next LTPS TFT because silicide source/drain is formed at low temperature. Several SB TFTs with mid-gap Schottky barrier height (SBH) have been reported, but devices need structure modification to avoid an ambipolar behavior [14–16]. There has been a few reports using specific metals having low SBH like yttrium, dysprosium for electron, platinum for hole, but more researches on SB TFTs are necessary for progress of 3D integration [17].

In this letter, we evaluated low temperature processes which are necessary for the fabrication of SB TFT. A low temperature oxide (LTO) capacitor is fabricated for tests as a gate dielectric, and a metal-induced lateral crystallization (MILC) is performed for poly-Si channel crystallization [8,18]. Finally 0.1 μm n-type SB TFT with erbium silicide source/drain having low SBH to electrons is demonstrated using these low temperature process.

2. Experimental details

An amorphous Si with 90 nm thickness was deposited on a thermally grown 150 nm oxide by low pressure chemical vapor deposition (LPCVD). A 0.1 μm active channel was defined by electron

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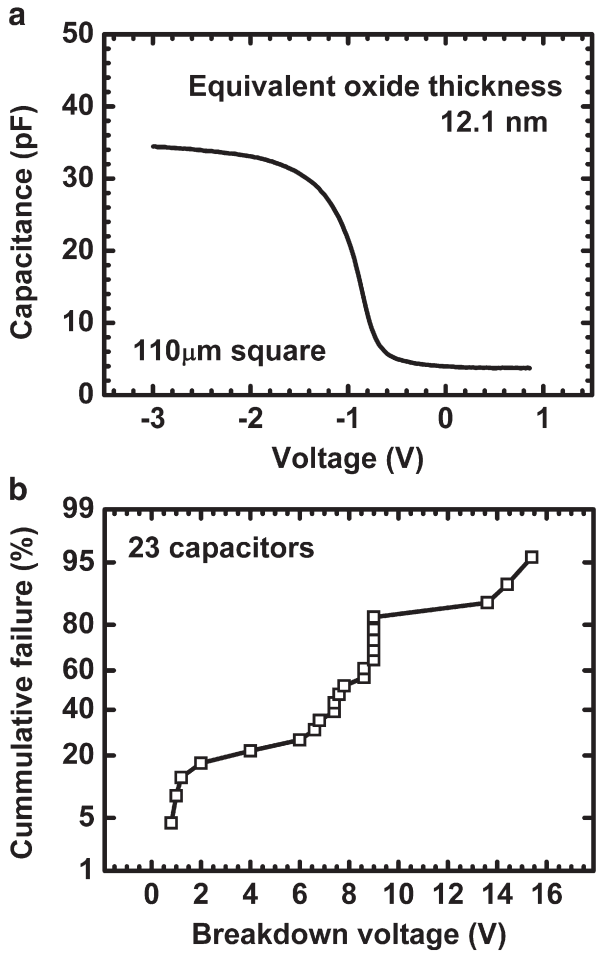

Fig. 1. (a) *C*–*V* and (b) leakage characteristics of fabricated capacitors using LTO dielectric.

beam lithography (EBL) and dry etching. After a LTO layer with a thickness of 13 nm was deposited as a gate dielectric at the rate of 1 nm/min by flowing SiH_4 and O_2 gas into LPCVD chamber at 400 °C, 70 nm thick poly-Si was deposited by LPCVD at 600 °C. The poly-Si was in-situ doped with phosphorus by adding PH_3 gas during the deposition. After 0.1 μm gate pattern was defined by EBL and dry etching, LTO layer was deposited and etched back for gate spacer formation. In order to crystallize an amorphous Si channel, nickel with a thickness less than 1 nm was deposited on whole area of the wafer by sputter and N_2-annealed at 500 °C for 20 h. Since the lattice constant of the nickel silicide formed outside the channel is similar with silicon, this nickel silicide induces a crystallization of amorphous silicon under gate electrode in a direction of channel. An erbium film of 50 nm was deposited by sputtering at high vacuum of 1×10^{-5} Pa after a dilute HF-dip and then wafers were annealed at 500 °C for 3 min below 1×10^{-4} Pa to prevent the oxidation of deposited metal. An erbium is chosen as source/drain metal of n-type SB TFT, because of its low SBH (0.28 eV) for electrons. The non-reacted erbium is removed by mixture of H_2SO_4 and H_2O_2, and wafers were sintered at 400 °C for 10 min in N_2 ambient before measurements. Throughout the whole processes, a temperature was kept as low as less than 600 °C.

The structures of fabricated SB TFT and the polycrystalline channel were analyzed by scanning electron microscope (SEM; FEI Sirion, acceleration voltage 10 kV) and scanning transmission electron microscope (STEM; Hitachi HD-2300A, acceleration voltage 200 kV) with sample preparation by focused ion beam (FEI Nova200). The electrical characteristics of capacitor and SB TFT were measured by Keithley 590 CV analyzer and HP4156B parameter analyzer.

3. Results and discussion

Fig. 1 shows a capacitance–voltage (*C*–*V*) characteristics and breakdown voltages of the MOS capacitor which is fabricated by depositing LTO dielectric and aluminium on 10^{15} cm^{-3} p-type Si substrate. As shown in Fig. 1(a) the capacitance curves falls sharply as voltage increases and there is no hysteresis. If the curve falls slowly, it means that many interface traps between a channel and a gate dielectric exist, so the trap density of a LTO gate dielectric is expected to be low. Equivalent oxide thickness is 12.1 nm similar to physical thickness of deposited LTO film. Fig. 1(b) shows the breakdown voltage characteristics of 23 LTO capacitors from a leakage current measurement by HP4156B. Most capacitors have a breakdown voltage of about 8 V with more than 1 A/cm^2 leakage current and the dielectric breakdowns occur at about 6.6 MV/cm. The breakdown field of thermal oxide is 9.5 MV/cm. Though it is not shown here, an auger electron spectroscopy result shows the atomic ratio of Si and O in the LTO film is 35:65 and equivalent to thermal oxide. Therefore this LTO film is suitable for the gate dielectric of low temperature SB TFTs.

Fig. 2 shows the SEM image of a poly-Si film crystallized by MILC after Secco etch. After formation of oxide dummy gate patterns on an amorphous Si wafer, a 5 nm thick nickel film was deposited and annealed for 20 h at 400 °C. Poly-Si grains with various shapes are confirmed after Secco etch due to etch rate difference between amorphous and polycrystalline Si. Poly-Si grains of the left side have random growing directions and shapes, and there are many holes etched away. On the other hand, grains of the right side, where the dummy gate once existed, are grown laterally in one direction and have fewer holes. This shows that the right-side MILC region has better poly-Si quality than left-side metal-induced-crystallization region. Using a MILC in low temperature fabrication of SB TFTs, poly-Si grains under the channel region grow in the same direction of the channel, and the mobility of electron carriers increases.

Fig. 3 shows the subthreshold characteristics (I_D–V_G) and drain current (I_D–V_D) of n-type SB TFT. The channel width and gate length are 0.1 μm as shown in inset of Fig. 3. As shown in Fig. 3(a), the device

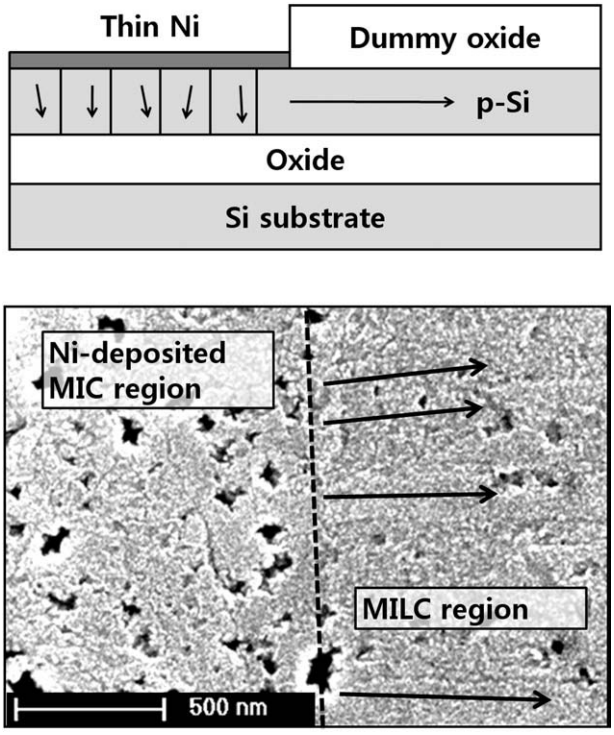

Fig. 2. A schematic cross-sectional structure and Si grain SEM image of amorphous Si crystallization using MILC.