Available online at www.sciencedirect.com
ScienceDirect
Thin Solid Films 517 (2008) 1204–1208
www.elsevier.com/locate/tsf

Application of fluorine doped oxide (SiOF) spacers for improving reliability in low temperature polycrystalline thin film transistors

Li-Wei Feng[a], Ting-Chang Chang[b,*], Po-Tsun Liu[c], Chun-Hao Tu[a], Yung-Chun Wu[d], Che-Yu Yang[a], Chun-Yen Chang[a]

[a] Institute of Electronics, National Chiao Tung University, Hsin-Chu, 300, Taiwan, ROC
[b] Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-set University, 70 Lien-hai Road, Kaohsiung 804, Taiwan, ROC
[c] Department of Photonics and Display Institute, National Chiao Tung University, Hsin-Chu, 300, Taiwan, ROC
[d] Department of Engineering and System Science, National Tsing Hua University, Hsin-Chu, 300, Taiwan, ROC

Available online 19 September 2008

Abstract

The novel process of self-aligned fluorine doped oxide (SiOF) spacers on low temperature poly-Si (LTPS) lightly doped drain (LDD) thin film transistors (TFTs) is proposed. A fluorine doped oxide spacers were provided to generate the lower dissociation Si–F bonds adjusted to the interface of the drain which is the largest lateral electric field region for lightly doped drain structure. The stronger Si–F bonds can reduce the bonds broken by impact ionization. It is found that the output characteristics of SiOF spacers TFTs show the superior immunity to kink effect. The degradations in Vth shifting, subthreshold slope, drain current and transconductance of SiOF spacers after DC stress are improved.

Keywords: Fluorine doped oxide (SiOF); Poly-Si; Thin film transistor (TFT); Lightly doped drain (LDD); Direct current (DC) stress

1. Introduction

The interest in low temperature polycrystalline silicon thin film transistors (LTPS-TFTs) has increased because of their wide applications on active matrix liquid crystal displays (AMLCDs) [1], organic light-emitting displays (OLEDs) [2], dynamic random access memories (DRAMs) [3], and static random access memories (SRAMs) [4]. This is because the field effect mobility in polycrystalline silicon is significantly higher (by two orders of magnitude) than that in amorphous silicon [5].

However, issue of poly-Si TFT is the main constraints toward the applications due to the granular structure of poly-Si which degrade performance and reliability. Moreover, a low process temperature, i.e. less than 600 °C, also produces numerous defects at the poly-Si\SiO_2 interface and polysilicon boundaries. There are many investigations about the improvement of the poly-Si TFTs reliability. One of the approaches is the passivation of the grain boundary traps by incorporating hydrogen [6–8] or fluorine ion [9–13] in LTPS-TFTs. It is reported that the introduction of fluorine passivation method would provide the better reliability due to its stronger dissociation energy of Si–F bonds.

However, most of the investigations were reported by using fluorine implantation into gate poly-Si, and implantation into channel poly-Si. It needs an extra implantation, which may cause the implantation damage and shifts the threshold voltage. It is known that hot carrier degradation is caused by the energetic electrons generated by impact ionization near the drain of the channel region [14]. So we introduce the self-aligned fluorinated silica glass (FSG) spacer technique to generate the higher dissociation Si–F bonds that adjust to the interface of the drain which is the largest lateral electric field region for lightly doped drain structure. Therefore, this method can achieve the improvement of reliability without any

* Corresponding author. Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, 70 Lien-Hai Rd. Kaohsiung, 80424, Taiwan, ROC. Tel.: +886 7 5252000x3708; fax: +886 7 5253709.
E-mail address: tcchang@mail.phys.nsysu.edu.tw (T.-C. Chang).

0040-6090/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2008.04.106

additional process step for a conventional top-gate lightly doped drain (LDD) polysilicon TFT structure. This work also can analyze the relationship of reliability behaviors between the fluorine ions in the sideward spacer region near drain side of channel and the defects formation under a DC bias stress.

2. Devices structure and fabrication

The fabrication of devices started by depositing a 50 nm undoped amorphous Si (a-Si) layer at 550 °C in a low-pressure chemical vapor deposition (LPCVD) system on Si wafers covered with a 500 nm thick thermal oxide layer. The a-Si layer was re-crystallized by solid-phase-crystallization (SPC) process in furnace at 600 °C for 24 h in a N_2 ambient. After patterning and etching the active region, the 50 nm thick SiO_2 (tetraethylorthosilicate) and the 200 nm thick poly-Si gate were both deposited by LPCVD system. After gate electrode formation, phosphorus ions at a dose of 5×10^{13} cm^{-2} and an energy of 17 keV were implanted to form the lightly doped source/drain regions and wafers were subjected to a rapid thermal anneal (RTA) at 820 °C for 20 s for dopants activation. Then the wafer was loaded into a plasma enhanced chemical vapor deposition (PECVD) system using the mixture gases of CF_4 and TEOS at 300 °C to grow a 300 nm thick FSG on the exposed gate and source/drain regions. For comparison, wafer with conventional TFTs was also processed on the same run by deliberately depositing only the TEOS oxide without fluorine dopants. Then the FSG layers and the conventional TEOS oxide were anisotropically etched by RIE to form the sidewall spacer abutting the poly-Si gate without additional mask. Phosphorus ions at a dose of 5×10^{15} cm^{-2} and an energy of 17 keV were implanted to form the n^+ gate, source/drain regions and were activated by RTA at 820 °C for 20 s also. The 500 nm thick TEOS oxide were deposited and patterned into the contact holes. The 500 nm thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned to form metal pads. Finally, the finished devices were sintered at 400 °C for 30 min in an N_2 ambient. In this study, all devices investigated have channel length of 3 μm and width of 10 μm. The device cross-section was shown in the inset of Fig. 2. In this work, a DC stress (Vgs=15 V, Vds=30 V) was applied for a maximum duration of 10^4 s to investigate the reliability behaviors.

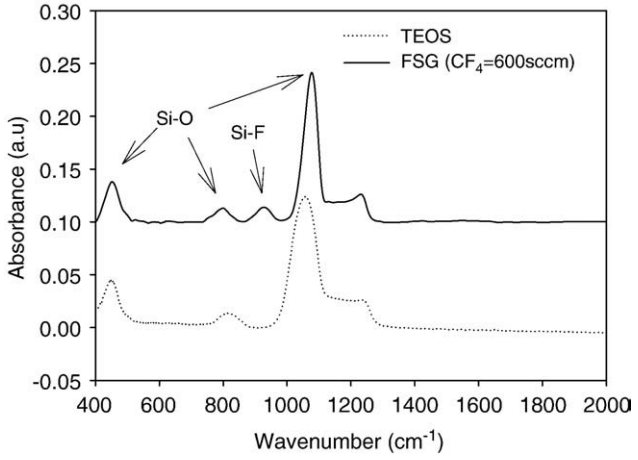

Fig. 1. FTIR spectra of FSG film and TEOS film between 2000 cm^{-1} and 400 cm^{-1}.

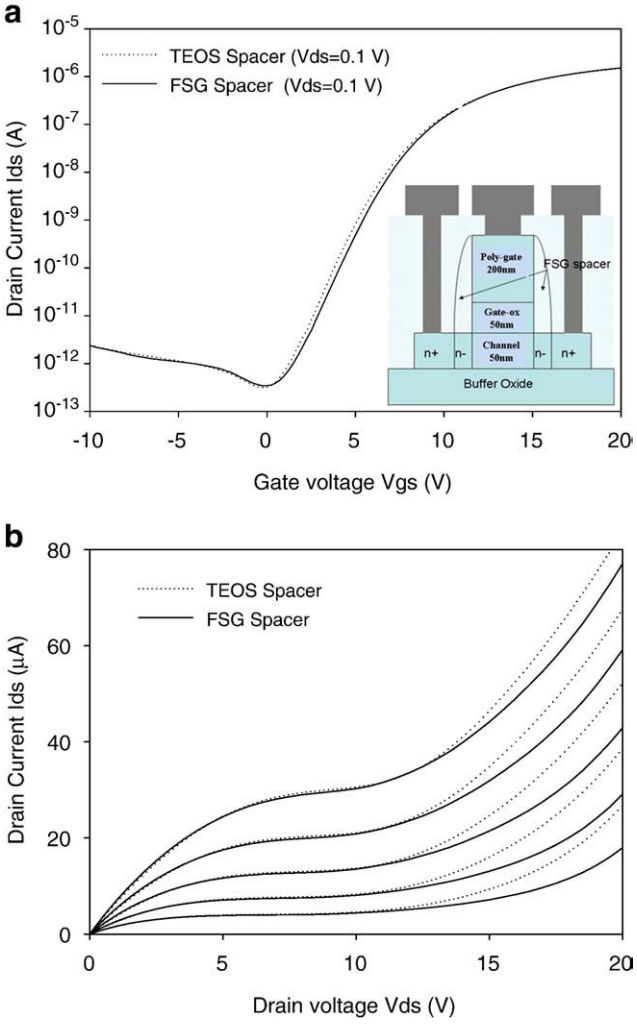

Fig. 2. Comparison of (a) Ids–Vgs characteristics of FSG spacer TFT and TEOS spacer TFT for Vds=0.1 V (inset is the schematic cross-section of the SiOF spacer TFT structure.) and (b) output characteristics for FSG spacer and TEOS spacer TFT, W/L=10 μm/3 μm, Vg–Vth=0, 1, 2, 3, 4 V.

3. Results and discussion

Fig. 1 shows the Fourier transform infrared (FTIR) spectra of undoped SiO_2 and FSG films between 400 cm^{-1} and 2000 cm^{-1}. The FTIR spectra were measured from an unpatterned wafer with undoped SiO_2 and FSG layer, respectively. The main peak of function group Si–F is around 930 cm^{-1}. The signal of Si–F bonds is clearly observed in the FSG film.

Fig. 2(a) and (b) shows the comparison of transfers and output curves for poly-Si TFTs with TEOS and SiOF spacer, respectively. It is found that the Ids–Vgs characteristics for Vds=0.1 V of transistor with W=10 μm and L=3 μm in both types of poly-Si TFTs were nearly the same. This indicates that the introduction of FSG spacer in poly-Si TFT device does not degrade electrical performance. In Ids–Vds characteristics for