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A TCAD simulation study of impact of strain engineering on nanoscale strained Si NMOSFETs with a silicon–carbon alloy stressor

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ABSTRACT

Stress distributions in the Si channel regions of silicon–carbon source/drain and stressed silicon nitride liner NMOSFETs were studied using the 3D ANSYS simulations. The mobility enhancement was found to be dominated by the tensile stress along the transport direction and compressive stress along the growth direction in wide devices. Stress along the width direction was found to have the least effect on the drain current in wide samples. Stress along the width slightly degraded the mobility gain in the narrow width regime. The compressive stress along the vertical direction, perpendicular to the gate oxide, contributes significantly to mobility enhancement and cannot be neglected in nanoscale NMOSFETs. The impact of width on performance improvements such as mobility gain was also analyzed using TCAD simulations.
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1. Introduction

Current silicon technologies use mechanical stress engineering to tailor band gap and carrier mobility to achieve performance enhancements. The device performance can be significantly improved with appropriately applied channel stresses [1]. Intentional stresses are introduced into the device channel using Silicon–Carbon (SiC) source and drain (S/D) stressors [2], a strained-silicon nitride cap layer (i.e. contact etching stop layer, CESL), and shallow trench insulation (STI) during the transistor fabrication process. However, the lattice mismatched SiC regions also induce stresses in the Si channel along the transverse (width) and vertical directions. This paper presents an analysis via simulation of the width dependence of the stress components (longitudinal, vertical and transverse) in the NMOS channel region, and its influence on mobility.

We performed a 3D simulation study [3,4] on the stress distribution in a strained Si channel and explored the impact of width on device performance indicators such as mobility gain. In Sections 2 and 3 we discuss the stress simulation, band structure model, and the mobility calculation used in our work. Section 4 discusses the results of the study. A summary is provided in Section 5.

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2. Stress simulation

The simulated process steps reflect common practices in the fabrication of stress-engineered transistors. The silicon wafer has the standard crystallographic orientation with a surface direction of (001) and a channel direction along [110]. The depth was 300 nm for STI. The recess depth for the SiC S/D stressor was 180 nm. The poly gate length was 55 nm and the poly gate height was 70 nm. For this paper, we studied the simplified 3D NMOS structure shown in Fig. 1. The Si channel was confined by epitaxially grown SiC in the S/D along the transport (x) direction and by STI in the transverse (y) direction. The whole structure was built on top of the Si substrate.

A well-developed process stress simulator, ANSYS [3], was used to calculate the stress distribution. The stress in the MOSFET channel region induced by the expansion of SiC was estimated by simultaneously solving equations of continuity and momentum balance with constitutive relations. Our mechanical simulations use the anisotropic law of Hooke to relate the stress tensor to the strain tensor via the three independent elastic constants ($C_{11}=167.5$ GPa, $C_{12}=65$ GPa and $C_{44}=80$ GPa for silicon; for nitride a value of $E=190$ GPa is used for Young's modulus and a value of $\nu=0.3$ for Poisson's ratio). In our process simulations, the stresses are computed as a function of the lattice mismatch between pure silicon and silicon carbon. To demonstrate the validity of our stress simulations, both experimental data from the IBM group [5] and simulation results for strained-silicon NMOS devices with a silicon–carbon S/D stressor are presented. Fig. 2 compares the spatial distribution of the lateral stress in the channel for the experimental data from the IBM group [5] and our simulation

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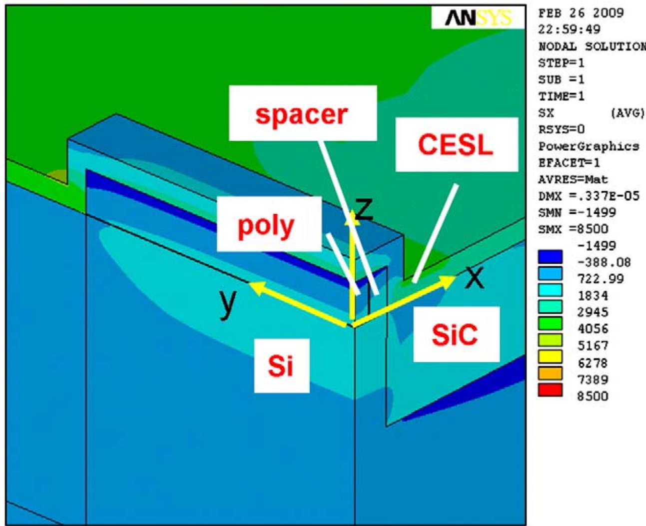

Fig. 1. Schematic NMOS device structure used in simulations. x denotes [110], y is [−110], and z is [001].

results. From Fig. 2, we see that our work is in good agreement with those extracted from the Convergent beam electron diffraction (CBED) measurements of the IBM group [5].

3. Band structure and mobility calculation

The longitudinal tension of the Si lattice in the channel region breaks the symmetry of the band structure, which lifts the degeneracy at the delta point of the conduction bands. This symmetry break also results in a decrease in electron effective mass along the transport (x) direction. Fig. 3 illustrates the conduction band structure of a 0.5 µm wide NMOSFET, calculated using a $sp^3d^5s^*$ empirical tight-binding model [6]. In addition to the benefit of a lower electron effective mass, the stress along the x and z directions (S_{xx} and S_{zz}) also causes a redistribution of carriers to the low effective mass sub-band valleys, resulting in reduced inter-band scattering in electron transport [7]. Subsequently, the electron mobility in the Si channel increases. To obtain the new mobility model for this study, we extended a simple model for the strain effect in the Si band [8], to include both shear strain and the quantum confinement effect in the inversion layer of NMOSFETs. Beginning with the Bir–Pikus effective Hamiltonian near

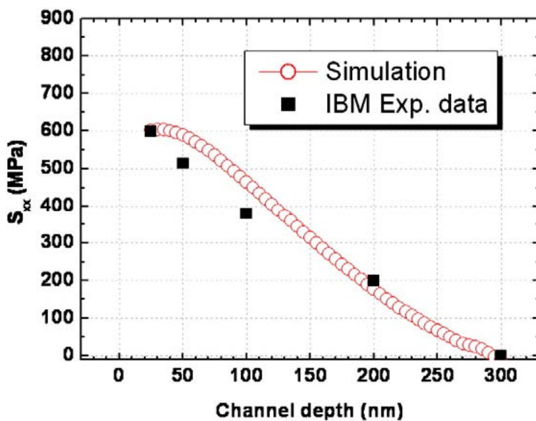

Fig. 2. The distribution of the lateral stress component in a transistor structure with SiC source/drain stressors for experimental data [5] and our simulation results. The agreement between experimental and simulation data is quite good.

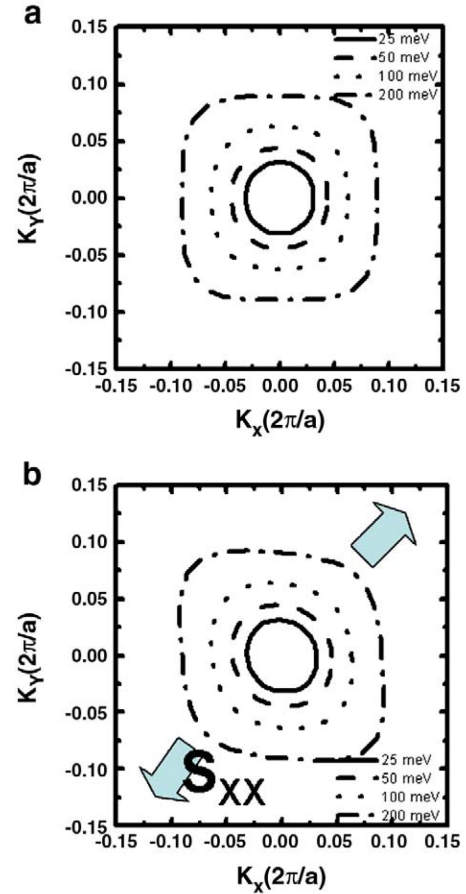

Fig. 3. Constant energy counters (units of eV) of lowest conduction band valley for (a) unstrained transistor and (b) transistor with SiC S/D and tensile-stress CESL. Both tensile S_{xx} and compressive S_{zz} result in the lowest effective mass along the transport direction. Note that units of K_X and K_Y are both $2\pi/a$.

the Δ point [9] and considering the Si crystal symmetry, the Hamiltonian of the z-valley is given by:

$$E_C^{[001]} = \frac{\hbar^2 K_Z^2}{2m_l(\varepsilon)} + \frac{\hbar^2 K_X^2}{2m_t^x(\varepsilon)} + \frac{\hbar^2 K_Y^2}{2m_t^y(\varepsilon)} + \frac{\hbar^2}{2m_0}\Xi_3\varepsilon_{xy}K_XK_Y + \frac{\hbar^2}{2m_0}[\Xi_2\varepsilon_{yz}K_ZK_Y + \Xi_2\varepsilon_{zx}K_XK_Z] + \Delta E_{\text{split}} \quad (1)$$

$$\Delta E_{\text{split}} = \Xi_d(\Delta_1)(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) + \Xi_u(\Delta_1)\varepsilon_{xx} + \Xi_1\varepsilon_{yz}^2 \quad (2)$$

where ΔE_{split} is the conduction band shift due to strain (refer to Eq. (1)). The 4th term is the origin of the difference between longitudinal piezo-coefficient π_l and transverse piezo-coefficient π_t in the [110] channel. The parameter Ξ_3, which is omitted in Ref. [8], expresses the dependence of effective mass on shear strain ε_{xy}. The lowest sub-band energy is expressed as $A_{\text{inv}}(m_0/ml)^{1/3}(qF_{\text{eff}})^{2/3}$ by the conventional quantum mechanism method for the inversion layer. Similarly, the lowest x-valley and y-valley sub-bands are given by $A_{\text{inv}}(m_0/ml)^{1/3}(qF_{\text{eff}})^{2/3}$. Considering the quantum confinement effect according to Refs. [10,11] the mobility tensor with a constant relaxation time approximation is given by:

$$\mu_{xx} = \frac{n_x}{m_t^x(\varepsilon)} + \frac{n_x}{m_l(\varepsilon)} + (1-4\Xi_3^2\varepsilon_{xx}^2)\frac{n_y}{m_t^y(\varepsilon)},$$
$$\mu_{yy} = \frac{n_x}{m_t^x(\varepsilon)} + \frac{n_y}{m_l(\varepsilon)} + (1-4\Xi_3^2\varepsilon_{yz}^2)\frac{n_x}{m_t^x(\varepsilon)}, \quad (3)$$
$$\mu_{xy} = 2\Xi_3\varepsilon_{xy}\frac{n_x}{m_t^x(\varepsilon)}$$

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